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Disha Malik

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32-bit Arithmetic Logical Unit (ALU) using VHDL

Disha Malik[1], Richa Singh Rathore[2]

[1]M. Tech Scholar, Department of ECE, Jayoti Vidyapeeth Women's University, Rajasthan, INDIA, dishamalik26@gmail.com

[2]M. Tech Scholar, Department of ECE, Jayoti Vidyapeeth Women's University, Rajasthan, INDIA, richasinghkgi@gmail.com

ABSTRACT

This paper involves the construction of 32-bit ALU (Arithmetic Logical Unit) using VHDL using Xilinx Synthesis tool ISE 9.2i and implementation them on FPGA (Field Programmable Gate Array) using Spartan 3E. The ALU is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs. The ALU performs mathematical, logical, and decision operations in a computer and is the final processing performed by the processor.

An Arithmetic unit does the following task:

- Addition
- Addition with carry
- Subtraction,
- Subtraction with borrow,
- Decrement
- Increment
- Transfer function.

A Logic unit does the following task:

- Logical AND
- Logical OR
- Logical XOR
- Logical NOT operation.

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Here, ALU is designed using VHDL (VHSIC hardware description language) is a hardware description language used in electronic design automation to describe digital and mixed signal systems such as field-programmable gate arrays and integrated circuits.

KEYWORDS- *FPGA, ALU, XILINX*

1. INTRODUCTION

Arithmetic Logic Unit, ALU is one of the many components within a computer processor. The ALU performs mathematical, logical, and decision operations in a computer and is the final processing performed by the processor. After the information has been processed by the ALU, it is sent to the computer memory. In some computer processors, the ALU is divided into two distinct parts, the AU (Arithmetic Unit) and the LU (Logical Unit). The AU performs the arithmetic operations and the LU performs the logical operations. In computing, an arithmetic and logic unit (ALU) is a digital circuit that performs integer arithmetic and logical operat ions. The ALU is a fundamental building block of the central processing unit of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs.

In the present day technology, there is an immense need of developing suitable data communication interfaces for real time embedded systems. Field Programmable Gate Array (FPGA) offers various resources, which can be programmed for building up an efficient embedded system. A Field-programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence it is named as "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL) VHDL (VHSIC hardware description language) is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field programmable gate arrays and integrated circuits.

The key advantage of VHDL, when used for systems design, is that it allows the behavior of the required system to be described

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(modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires). Another benefit is that VHDL allows the description of a concurrent system. VHDL is a dataflow language, unlike procedural computing languages such as BASIC, C, and assembly code, which all run sequentially, one instruction at a time. VHDL project is multipurpose and portable. Being created for one element base, a computing device project can be ported on another element base, for example VLSI with various technologies.

1.1 BLOCK DIAGRAM

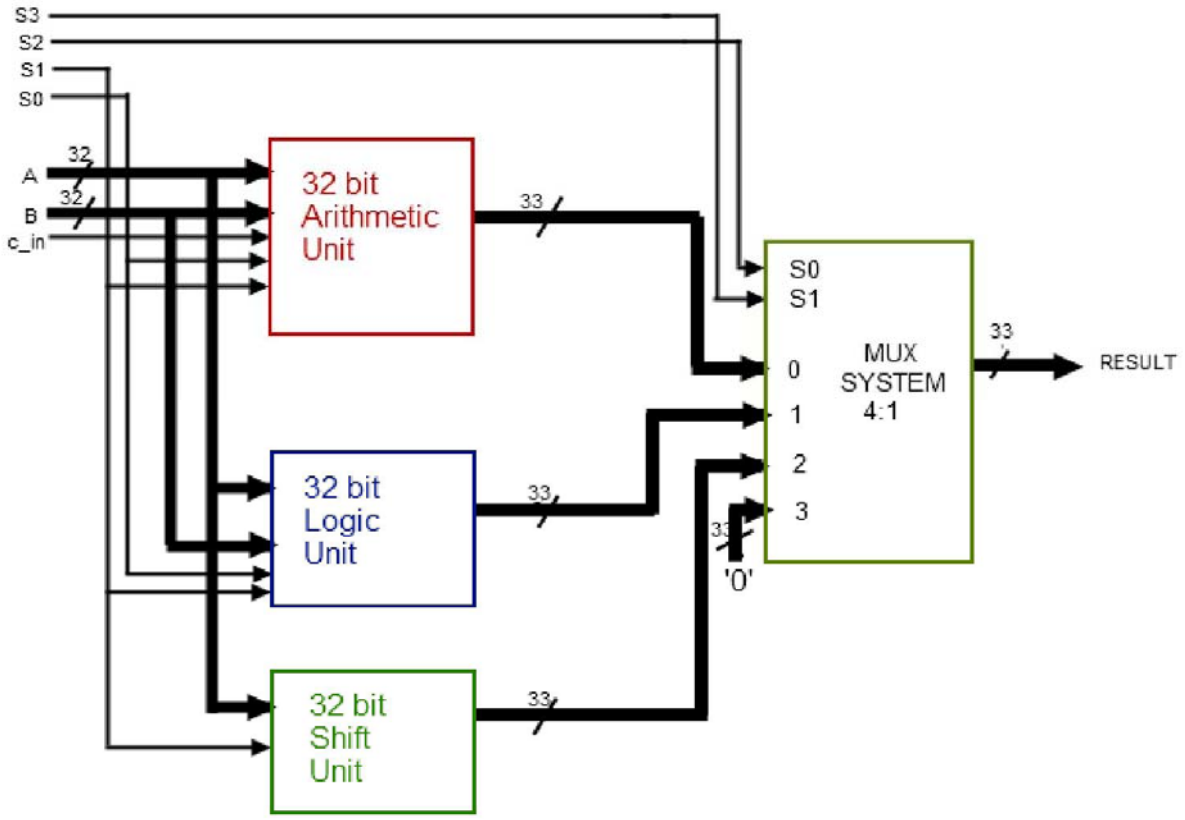

Figure 1: Block Diagram of 32-Bit ALU

2. DESIGN OF 32- BIT ALU

When designing the ALU we will follow the principle "Divide and Conquer" in order to use a modular design that consists of smaller, more manageable blocks, some of which can be re-used. Instead of designing the 4-bit ALU

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as one circuit we will first design one bit ADDER, SUBTRACTOR, OR, AND, NOT, XOR, LEFT SHIFT, RIGHT SHIFT UNIT. These bit-slices can then be put together to make a 32-bit ADDER, SUBTRACTOR, OR, AND, NOT, XOR, LEFT SHIFT, RIGHT SHIFT UNIT.

3. MODULES DESIGN OF 32-BIT ALU

3.1 32-BIT ARITHMETICUNITS

An Arithmetic unit does the following task: Addition, Addition with carry, Subtraction, Subtraction with borrow, Decrement, Increment and Transfer function. At first we start with making one bit Full Adder, then a 4-bit Ripple Carry Adder using four numbers of Full Adder and at last a 32-bit Ripple Carry Adder using eight numbers of 4-bit Ripple Carry Adder. Then designed thirty two numbers of single-bit 4:1 Multiplexer. The circuit has a 32-bit parallel adder and thirty two multiplexers for 32-bit arithmetic unit. There are two 32-bit inputs A and B and 33-bit output is RESULT. The size of each multiplexer is 4:1. The two common selection lines for all thirty two multiplexers are So and S1.C-in is the carry input of the parallel adder and the carry out is C-out. The thirty two inputs to each multiplexer are B- value, Complemented B-value, logic-0 and logic-1.The output of the circuit is calculated from the following arithmetic sum:

RESULT = A + Y + C-in

Where A is a 32-bit number, Y is the 32-bit output of multiplexers and C-in is the carry input bit to the parallel adder.

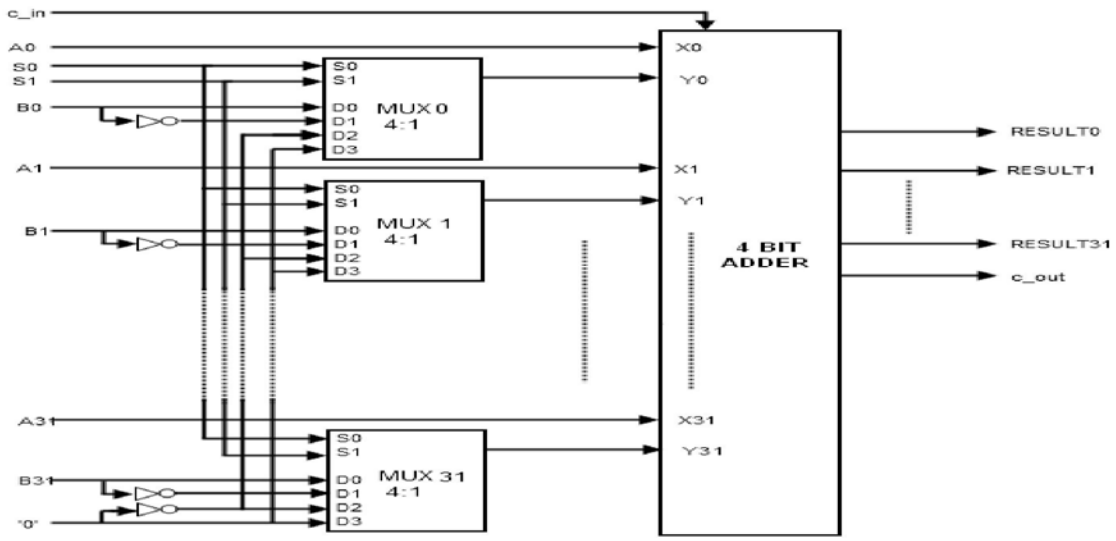

Figure 2: 32-Bit Arithmetic Unit

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4. SIMULATED TIMING DIAGRAM OF ARITHMETIC UNIT

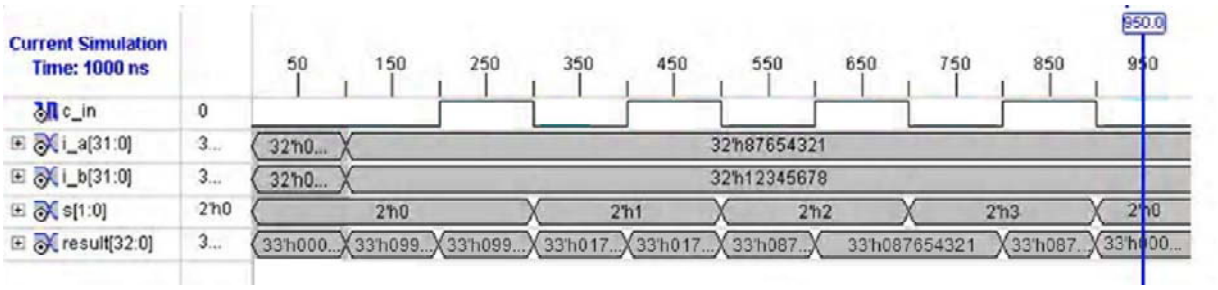

Figure 3: Timing Diagram

4.1 32-BIT LOGIC UNIT

A Logic unit does the following task: Logical AND, Logical OR, Logical XOR and Logical NOT operation. We design a logic unit that can perform the four basic logic micro operations: OR, AND, XOR and Complement, because from these four micro-operations, all other logic micro-operations can be derived. The logic unit consists of four gates and a 4:1 multiplexer. The outputs of the gates are applied to the data inputs of the multiplexer. Using to selection lines S0 and S1 one of the data inputs of the multiplexer is selected as the output. For a logic unit of 32-bit, the output will be of 33-bit with 33th bit to be High-impedance. The common selection lines are applied to all the stages.

4.2 SIMULATED DIAGRAM OF LOGIC UNIT

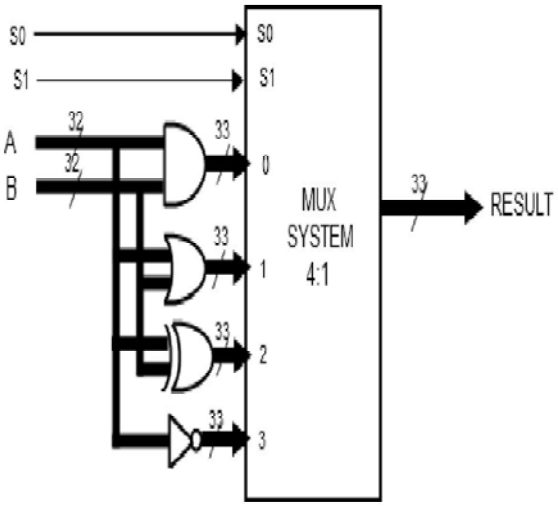

Figure 4: Simulated Diagram of Logic Unit

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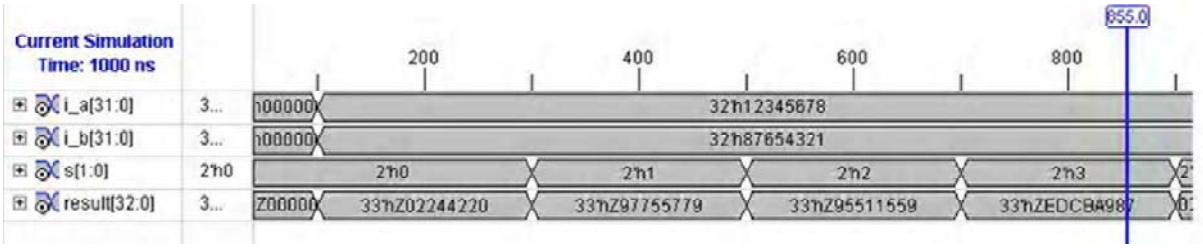

Figure 5: Timing Diagram

4.3 32-BIT SHIFTER UNIT

Shifter unit is used to perform logical shift micro-operation. The shifting of bits of a register can be in either direction- left or right. The content of a register that has to be shifted first placed onto common bus. This circuit uses no clock pulse. When the shifting unit is activated the register is shifted left or right according to the selection unit. For a shift unit of 32-bit, the output will be of 33-bit with 33th bit to be the outgoing bit.

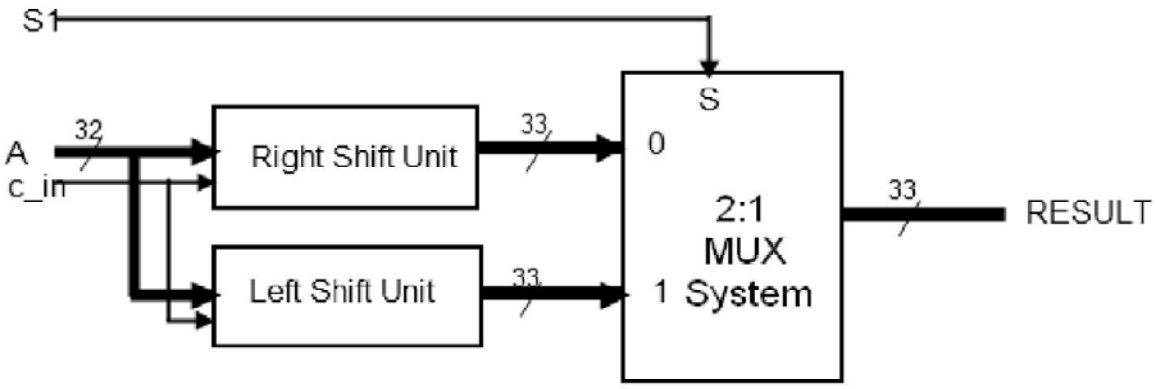

Figure 6: Block Diagram of Shift Unit

4.4 SIMULATED TIMING DIAGRAM OF SHIFTER UNIT

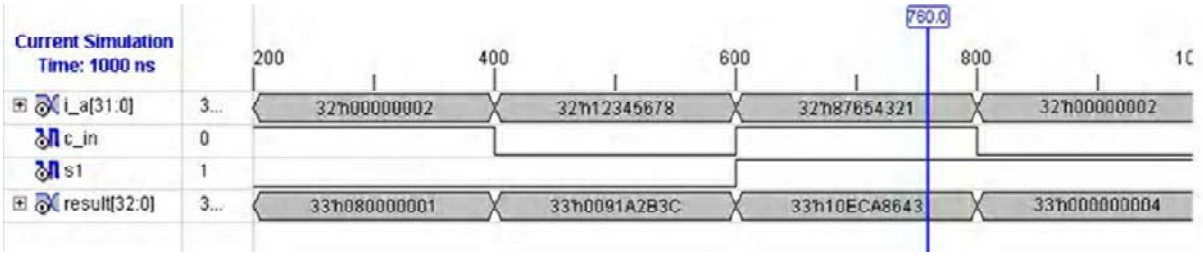

Figure 7: Timing Diagram of Shifter Unit

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4.5 FUNCTION OF ALU:

S3	S2	S1	So	C-in	RESULT	Operation
0	0	0	0	0	A+B	Addition
0	0	0	0	1	A + B + 1	Addition with carry
0	0	0	1	0	A + B	Subtraction with borrow
0	0	0	1	1	A + B + 1	Subtraction
0	0	1	0	0	A – 1	Decrement
0	0	1	0	1	A	Transfer
0	0	1	1	0	A	Transfer
0	0	1	1	1	A + 1	Increment
0	1	0	0	x	A·B	AND
0	1	0	1	x	A+B	OR
0	1	1	0	x	A⊕B	XOR
0	1	1	1	x	NOT A	Complement
1	0	0	x	x	LSR A	Shift Right
1	0	1	x	x	LSA A	Shift Left

5. SPARTAN-3E FPGA FEATURES AND EMBEDDED PROCESSING FUNCTIONS

The Spartan-3E Starter Kit board highlights the unique features of the Spartan-3E FPGA family and provides a convenient development Board for embedded processing

applications. The board highlights these features:

Spartan-3E FPGA specific features:

- Parallel NOR Flash configuration
- Multi-Boot FPGA configuration from Parallel NOR Flash PROM
- SPI serial Flash configuration

Embedded development

- Micro-Blaze™ 32-bit embedded RISC processor
- Pico-Blaze™ 8-bit embedded controller
- DDR memory interfaces

6. CONCLUSION

In our paper "Design and Implementation of a 32-bit ALU on Xilinx FPGA using VHDL" we have designed and implemented a 32 bit ALU. Arithmetic Logic Unit is the part of a computer that performs all arithmetic computations, such as addition and subtraction, increment, decrement, shifting and all sorts of basic logical operations. The ALU is one component of the CPU (Central Processing Unit).

Here, using VHDL we have designed a 32 bit ALU which can perform the various arithmetic operations of Addition, Subtraction, Increment, Decrement, Transfer, logical operations such as AND, OR, XOR, NOT and also the shift operation.

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8. BIOGRAPHY

	Disha Malik did her B.tech in ECE from G.L.Bajaj Institute of Technology and Management Greater Noida. She is pursuing M.tech in VLSI from JVWU. Her area of interest are Digital Image processing, Digital Computer Networking, VHDL etc.
	Richa SinghRathore did her B.tech in ECE from Krishna Girls Engineering College Kanpur. She is pursuing M.tech in VLSI from JVWU. Her areas of interest are Digital Image Processing, Microelectronics, Intergated Circuit etc.