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# Accomplishment and Timing Presentation: Clock Generation of CMOS in VLSI

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## Abstract

Accomplishment independent timing issues in an oversampled system. This research paper present the oversampled input receiver accomplishment details and measured time results. The first section of this paper provides an impression of the sampling system included on the test chip. The timing accurateness is mainly bounded by the clock generators. This includes interpolation circuits for creating finely spaced clocks and architectural trade-offs for structure multiphase clock generators with tunable production or output phases. The research concludes with test results for static phase and compensation techniques for two clock generators. Having explored methods to build clock generators. Then examines clocked input samplers that can imprison high-speed signals while having a minimal impact on timing accuracy.

***Key Word:*** *S-RAM, Bandwidth, Clock Generators, PMOS, CMOS, DLL, PLL.*

## 1. Introduction

To better appreciate the trade-offs and to test the compensation methods, a sampling receiver test chip designed and measured. A building block diagram of the test chip is shown in Figure 1.1. The part is made-up in a standard0.25µm, five metal layer processes. It contains eight sampling channels that feed either an S-RAM memory or an on-chip histogram counter. The sampling rate per channel is 46 G samples/s with a 900MHz reference clock and 50 sampling phases [1]. The eight sampling channels generate 388 GB/s of digital data but to reduce the required bandwidth of the acquisition memory, the data rate is reduced by oversampling only half the cycle. The memory is accomplished of storing the resulting 244 GB/s data stream with no supplementary loss of information. The chip contains two circuits that can be used to generate the finely spaced (37ps)

clocks. One uses a delay line with interpolation and the other uses an array of oscillators [2].

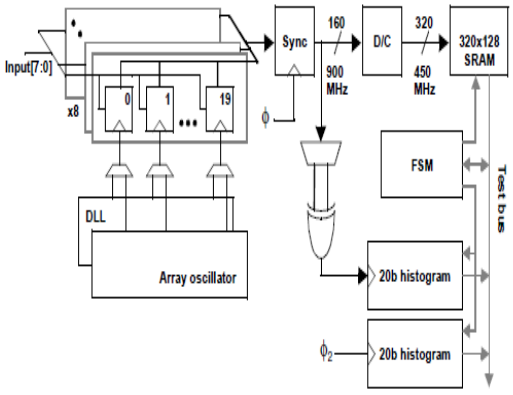


**Figure 1.1:** Block diagram: Testing of chip for SRAM Memory

## 2. Clock Generation

The clock generators drive the input sampling receivers and set the timing of the whole system. To compare design trade-offs and performance, both a phase-locked loop and delay-locked loop were included on the test chip. The performance of the delay elements in the clock generators appreciably impacts the jitter performance, so this section starts with a description of a low-jitter differential delay element [3]. The delay element is then changed into a tunable interpolator to permit fine phase spacing. The section continues with a discussion of the issues involving the amalgamation of tunable interpolators into a delay line and VCO to achieve a large modification range without compromising performance. The control loops and clock buffers are then described by the side of techniques to minimize the static phase offsets and jitter caused by these elements [4].

## 3. Basic Elements in Buffer

The clock generators are implemented with Maneatis style self-biased control loops and replica biased, variable delay, differential buffers with symmetric loads [5]. A buffer shown in Figure 2. The two PMOS devices that form the load structures are termed symmetric loads. If the output swing is equal to the bias voltage Vbp, then the resistance of the loads is symmetric about the crossing of the differential outputs. This reduces the jitter caused by common-mode provide clatter such as noise [6].

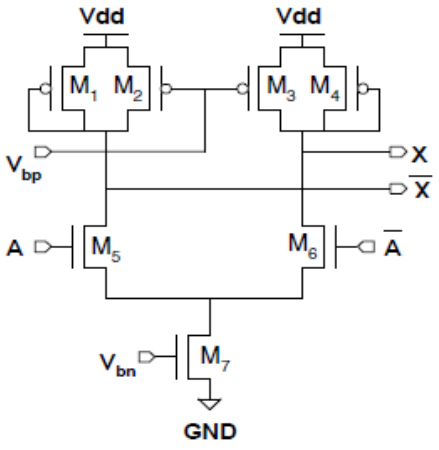


**Figure 1.2:** Differential delay element for buffer

Vbp is drive by the control loop to set the delay of the buffer. Vbn is energetically position by the replica biasing circuit in Figure 1.3 to set the output signal move backward

and forward equal to Vbp which maintain the symmetric environment of the loads. The degree of difference topology, symmetric loads, and replica biasing yields a delay element with a low understanding to supply clatter such as noise. A typical inverter has a delay understanding of approximately 1, while this element has a delay understanding of about 0.05, which is an enhancement by a issue part of twenty.

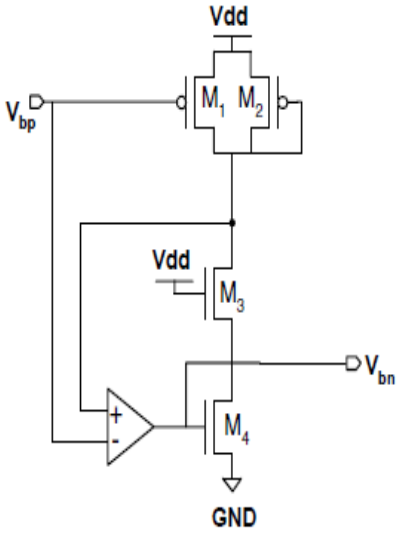


**Figure 1.3:** Replica bias generator for delay elements

## 4. Delay-Line Based Clock Generator

The central part of the delay line is five differential delay elements. Interpolators split the five clock phases into twenty differential clocks. A single level of interpolation, as shown in Figure 1.4, minimizes jitter because it minimizes the delay through the clock paths as compared to techniques using multiple levels of interpolation [5]. The interpolation ratios are chosen to maximize the adjustment range of all the interpolators. Nevertheless, this topology is unsatisfactory because the interpolators on the ends have a limited adjustment range of 1/8 a buffer delay one direction since their supposed position is within 12.5% of one of the input phases. To maintain a reasonable adjustment range, not only do the inputs to the interpolator need to have sufficient phase spacing, but the nominal weighting of the interpolators must not be exceptionally off-center from 1/2.

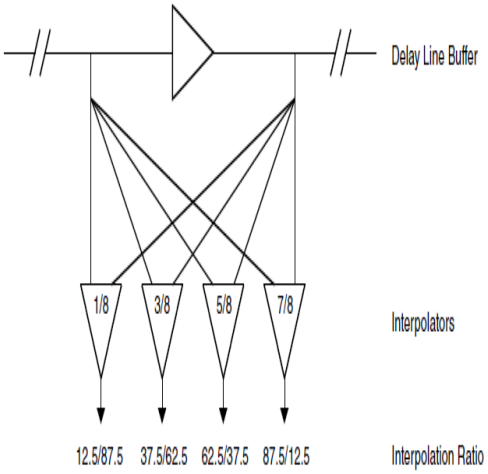


**Figure 1.4:** Initial exclamation plan for DLL

The modification range can be greater than before, at the cost of better jitter, by using two levels of interpolation, as shown in Figure 1.5 (a & b) . The design in Figure 1.5 (a) interpolates with a 50%/50% ratio between existing clock phases to generate new phases. The interpolators with the shorted inputs delay the existing phases so they are properly

interleaved with the new phases. An alternate technique is to synthesize both of the new phases via interpolation as shown in Figure 1.5 (b) which is identical to the original design shown in Figure 1.4 except with only two interpolators rather than four. Topology (a) has enhanced phase spacing in the presence of interpolation ratio errors as only half the phases are affected, but the interpolators with their inputs shorted in design (a) have no adjustment range. Topology (b) can have twice the DNL as (a) because the inputs to every other interpolators are reversed so adjacent phases are pushed in opposite directions. However, the interpolators in (b) do have a larger adjustment range of at least 0.25 of aFO-4 delay.

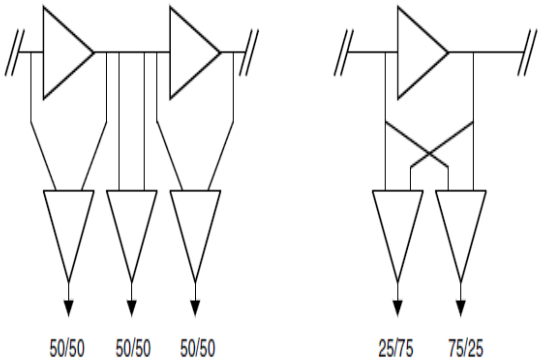


**Figure** 1.5 (a & b)**:** Interconnect techniques for phase interpolation.

## 5. Ring Oscillator Based Clock Generator

The before described interpolation techniques are also applicable to a conventional ring oscillator based VCO. Yang describes such a clock generator in with 24 phases for over sampling a 2.5 Gb/s SONET signal. However, given the need for interpolation, possibly a more interesting architecture is the array oscillator as described by Maneatis in. This structure uses multiple, coupled ring oscillators to create equally phase shifted clocks [7]. To those unknown with an array oscillator, the operation can be confusing so it is briefly reviewed before proceeding with the details of adding phase tuning to the structure. First, consider a series of uncoupled ring oscillators as shown in Figure 1.6. In an ideal environment, the ring oscillators will oscillate with identical frequencies, but with an arbitrary phase alignment. While this produces multiple output clocks, the arbitrary phase alignment of the clocks makes this solution uninteresting. To generate equally spaced output clocks, a forced phase alignment between the rings is required. This can be achieved by replacing each of the single input buffers with a two-input interpolator and coupling the rings together.

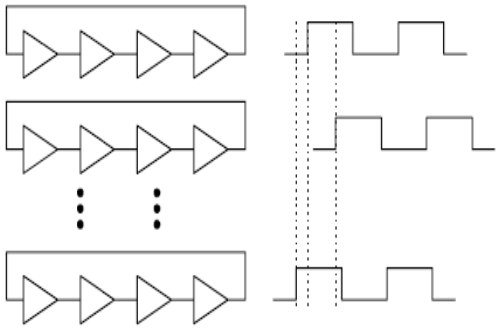

**Figure 1.6:** Multiple uncoupled ring oscillators

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## 6. Clock Drivers for DLL and PLL

Because the buffer and interpolator cells are low-swing, the clock signals need to be transformed to full-swing previous to driving the samplers. The level converter and clock buffers used in both the DLL and PLL are shown in Figure 1.7. In the course of sharing the circuit and making a last-minute sizing change in the array oscillator, the current source in the differential pair was mis-sized in the PLL [5]. The result was insufficient current to fully swing the input to the first inverter, and correspondingly, marginal clock signals. Fortunately, a few of the clock outputs did function sufficiently to obtain jitter measurements presented later in this chapter. However, phase spacing measurements were not possible.

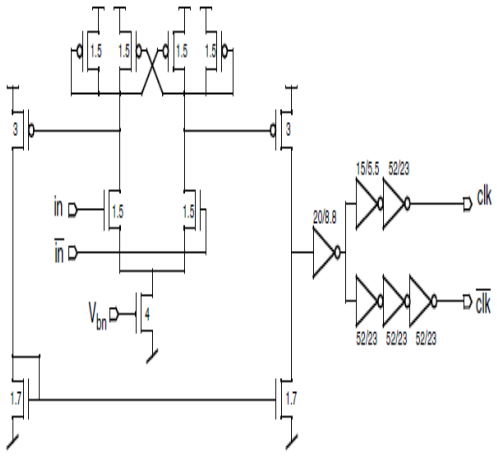


**Figure 1.7:** Low-to-high swing converter and clock buffers

The delay through the converter roughly tracks that of the delay elements in the clock generators because the differential pair is biased with same signal, Vbn. This biasing also implies that the slew rate of the input to the first inverter is also related to the operating frequency. At first glance, this appears fine; the rise and fall times remain roughly a constant percentage of the cycle time. However, this also means that the jitter scales with the clock period. A better solution is to bias the differential pair with a fixed current so that the current mirror is fast and the speed is independent of the frequency of the clock generator.

## 7. Measurement of Phase Results

Tunable interpolators in the clock generators make possible static tuning of clock phase offsets. To as it should be program the interpolators, the static phase spacing of the clocks have got to first be measured. The test chip multiplexes sampler outputs into a single counter to avoid the need for separate counters on each set of adjacent phases [8]. This makes the measurement process longer because the size of the bins can no longer be measured in parallel, but instead must be measured sequentially. Nevertheless, the measurement can be performed in less than a few seconds. A secondary measurement capability is provided by a clock multiplexer and output driver. Figure 1.8 shows the histogram counter and multiplexers as

implemented on the test chip. Because the input clocks to the histogram counter always consist of an even and odd clock, the multiplexers can be simplified by making one select between the even clocks and the other select between the odd clocks.

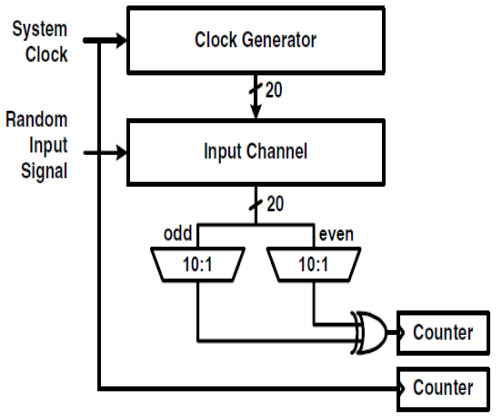


**Figure 1.8:** Architecture for histogram measurements of phase offsets

A 20-bit counter counts system cycles so that each histogram runs for an equal period of time. The counters are implemented as linear feedback shift registers (LFSR) to simplify design and minimize the area required compared to a regular binary counter. Decoding the LFSR count into a binary value is performed off-line by a workstation [9].

## 8. Conclusion

Static phase errors, timing jitter, sampler input offset voltage, and input capacitance are the primary challenges of implementing a CMOS oversampled receiver with high timing accuracy. Because of aggressive CMOS scaling, the most abundant resource available to address these problems is transistors. Static phase compensation is probably the most robust of the implemented techniques and results indicate that placing the nominal position of a clock edge to within a couple picoseconds is feasible. The phase tuning algorithm is driven by histogram counters that precisely measure phase offsets without introducing additional timing errors. In the test chip, the primary limitation to uniform phase spacing appears to be the complexity and size of the current-mode digital to- analog converters used in the interpolators.

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