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# VLSI DESIGN OF LOW POWER BARREL SHIFTER USING PSUEDO DYNAMIC (PDB) LOGIC

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## 1. INTRODUCTION

Barrel shifter is essential components in ALU. Barrel shifter is often used for shifting operation like shift right logical, shift left logical, shift left arithmetic, shift right arithmetic, right rotate, left rotate. The architecture of barrel shifter can be designed by using 2:1, 4:1, 8:1, 16:1 MUX trees. Barrel shifter is most essential element in DSP applications. Barrel shifter is designed using MUX trees to use it in repetitive form so that power consumed by the barrel shifter should minimum. The work is divided into two sections. At first, the multiplexer is designed using True single phase clock (tspc) and, by using MUX block barrel shifter is designed. Secondly, the multiplexer is designed using Pseudo dynamic logic (pdb) and, by using MUX block barrel shifter is designed. Result comprises of comparison of both technology techniques and simulation of above all logics which is helpful in low power ALU design.

## 2. INTRODUCTION TO BARREL SHIFTER

The Barrel shifter is the circuit block in the processor that shifts the data by specified number of bits. The shifter is designed to shift data bits logically and arithmetically either left or right. In logical left shift, the barrel shifter will shift the data bits by specified number of bits to more significant positions and the result has lower significant bits that are filled with zeros. In logical right shift, the barrel shifter will shift the data bits by specified number of bits to lower significant bits and the result has higher significant bits that are filled with zeros. The main circuit block for the barrel shifter is build based on the multiplexer circuit. Basically, a barrel shifter works to shift data by incremental stages which avoids extra clocks to the register and reduces the time spent shifting or

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rotating data (the specified number of bits are moved/shifted/rotated the desired number of bit positions in a single clock cycle). A barrel shifter is commonly used in computer-intensive applications, such as Digital Signal Processing (DSP), and is useful for most applications that shift data left or right-a normal style for C programming code. Rotation (right) is similar to shifting in that it moves bits to the left. With rotation, however, bits which "fall off" the left side get tacked back on the right side as lower order bits, while in shifting the empty space in the lower Barrel Shifter contains repeated blocks of 2x1 multiplexer and each multiplexer block is implemented using TSPC and PDB dynamic logic. Such logic styles are efficient in reducing power consumption as they avoid precharge pulse propagation. The voltage at the output of the dynamic circuit is stored on a parasitic capacitance, which is typically buffered before it is sent to the next stage. This temporary voltage is affected not only by charge sharing of the internal parasitic capacitances but also by the consequent dynamic circuit. Normally, a buffer at the output of the dynamic logic is required to drive the next stage. Since the output of the dynamic gate is sampled on parasitic order bits after shifting is filled with zeros .Data shifting is required in many key computer operations from address decoding to computer arithmetic. Full barrel shifters are often on the critical path, which has led most research to be directed toward speed optimizations. With the advent of mobile computing, power has become as important as speed for circuit designs. In this project we present arrange of 32-bit barrel shifters that vary at the gate, architecture and environment levels.

## 3. BARREL SHIFTER LOGIC

capacitances, periodic precharge phases of the output node are required. Additionally, these precharge pulses introduce extra noise in the gate and the propagation of these pulses through the static buffer result in extra power consumption. Fig. 1 shows the block diagram of a 3-stage barrel shifter with inputs x0-x7 and output z0-z7 (left shifter), and each row represents a stage. It consists of 2x1 multiplexers arranged into three rows with 8 multiplexers per row. Each row of multiplexer has common select line where s0 feeds the first row, s1 second and s2 third. A 1 in the first row (s0=1) represents a shift of one bit to the left. When s1=1 data is shifted by 2 bits,

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when s2=1 data is shifted by 4 bits .When any of the shift control bits are zero, data is passed unchanged through the row of multiplexers to the next row.

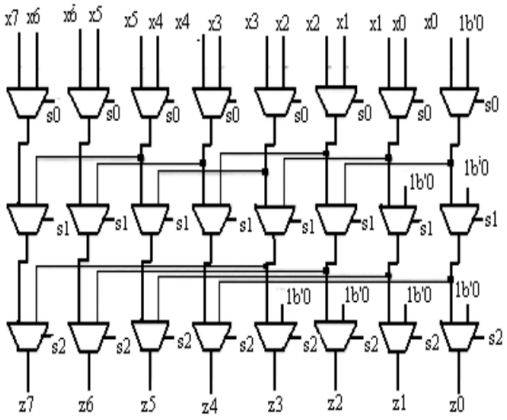


Figure 1: An 8 bit Left Barrel Shifter

## 3.1 MULTIPLEXER USING TSPC DYNAMIC LOGIC

The first single-phase clock policy was only introduced by Ji-Renet al. called the true single-phase-clock (TSPC). It overcomes the problem of precharge pulse propagation using NC2MOS or PC2MOS, as shown in Fig.2, but at the expense of an extra transistor as compared to a domino gate. In this gate, the dynamic node Z is precharged high and M9 is disabled.

As a result, the output Out holds its previous value. This circuit requires 3 clock transistor and it increase the load capacitance of the clock signal and thus the power consumption.

The implementation of multiplexers for barrel shifter is shown in Figure 2 and Figure 3.

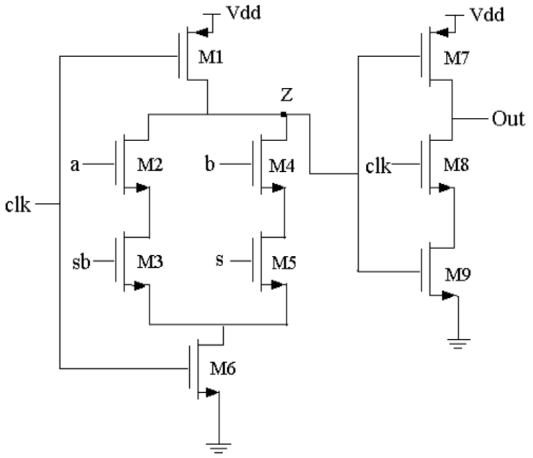


Figure 2: 2x1 multiplexer using tspc dynamic logic

## 3.2 MULTIPLEXER USING PDB LOGIC

Using this pseudo dynamic structure (PDB), the precharge pulse is blocked at the input of the buffer and is prevented from being propagated to the output of the dynamic gate. As a consequence, the power typically consumed in the buffer during the precharge phase is saved. Additionally, compared to TSPC-based dynamic logic, in this logic the clock transistor count is reduced from 3 to 2. As a result, the power consumption is significantly reduced due to lower load capacitance on the clock bus. In this circuit the source of output buffer transistor M8 is connected to node N instead of Gnd as shown in Fig.3. Using such a circuit topology, the value at node Z cannot propagate to the output

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Out during the precharge phase of the gate since during this phase, the evaluation transistor M6 is turned off.

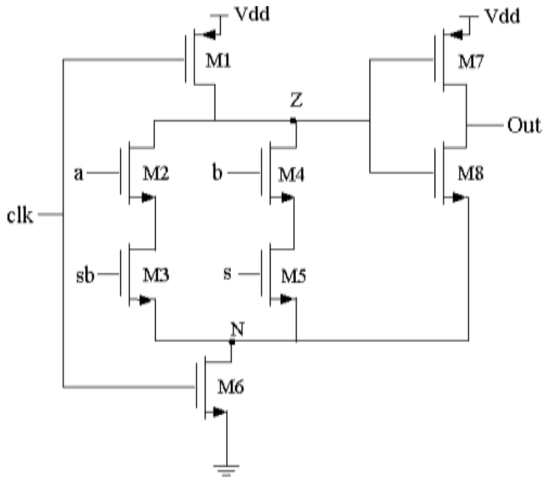


Figure 3: 2x1 multiplexer using PDB dynamic logic

## 4. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

All the circuits are simulated on mentor graphics pyxis schematic tool which provides a powerful and easy-to-use design entry environment with advanced capabilities that boost designer productivity. It gives platform to create, develop, simulate, verify, optimize and implement even the most challenging full custom analog and mixed-signal IC designs quickly and accurately.

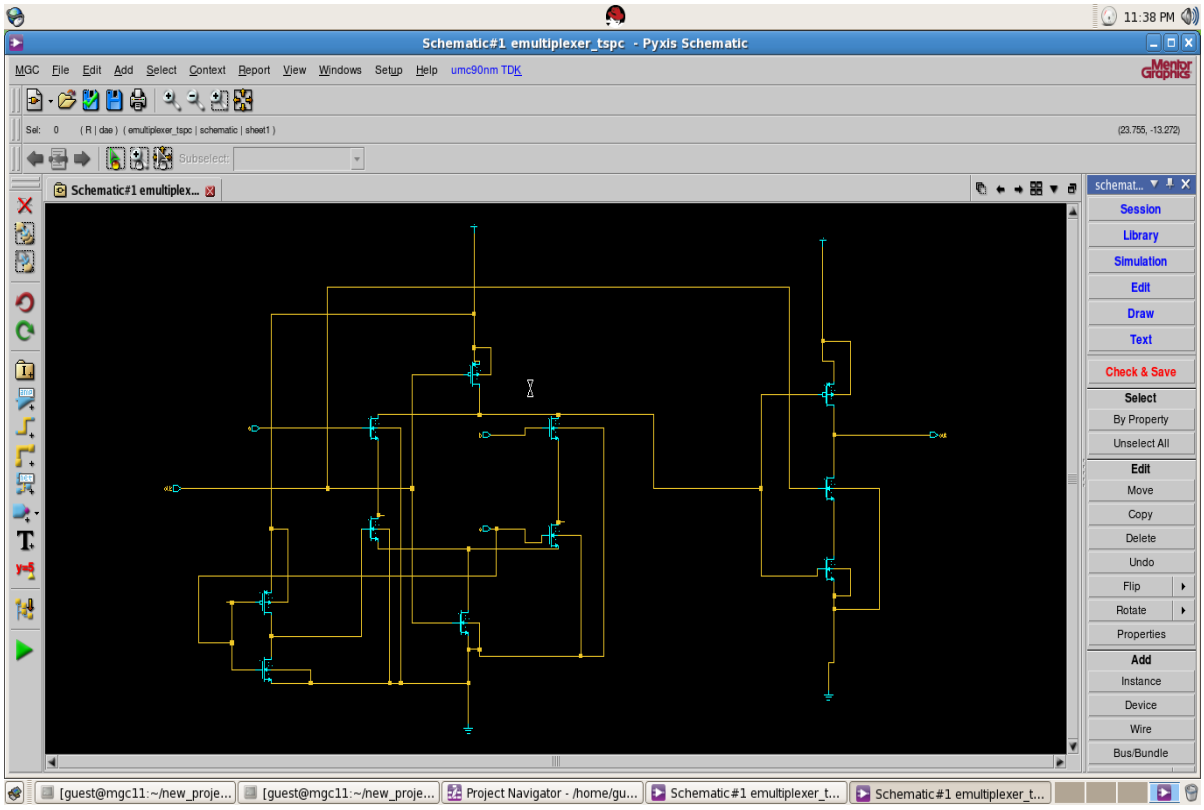


Figure 4: 2x1 schematic of multiplexer using tspc logic

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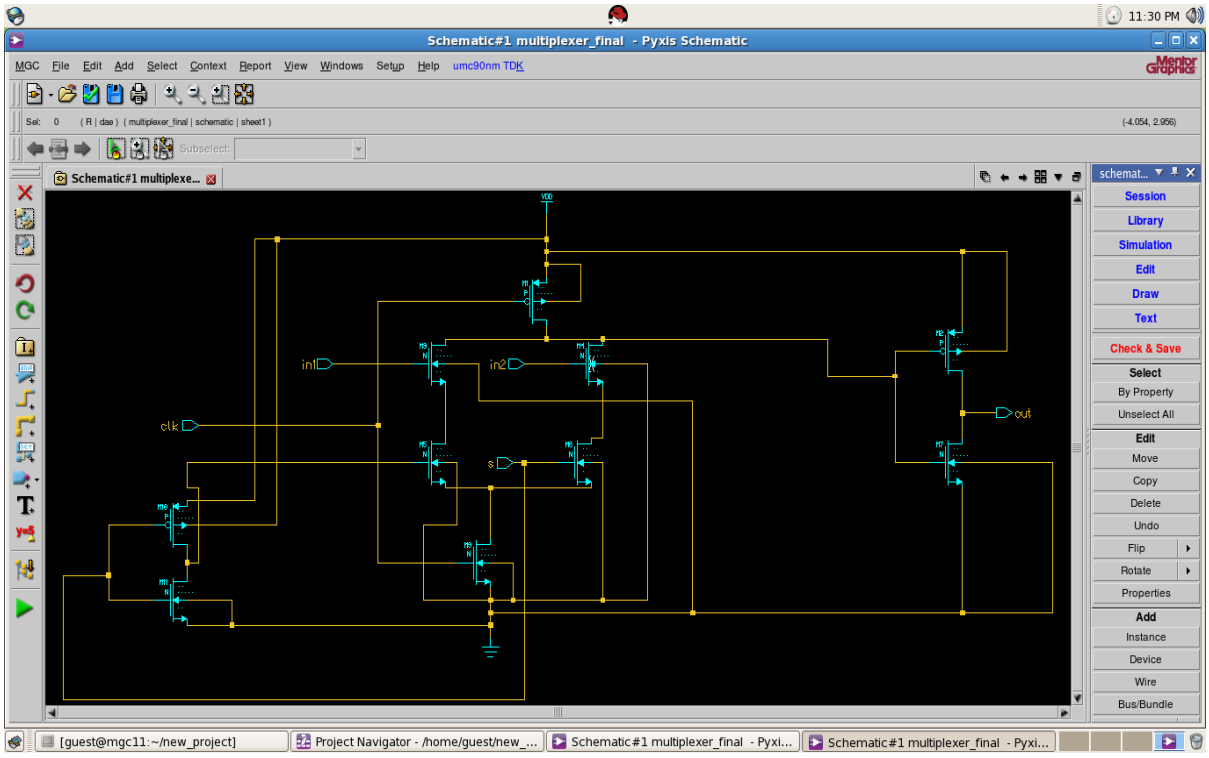


Figure 5: 2x1 schematic of multiplexer using pdb logic

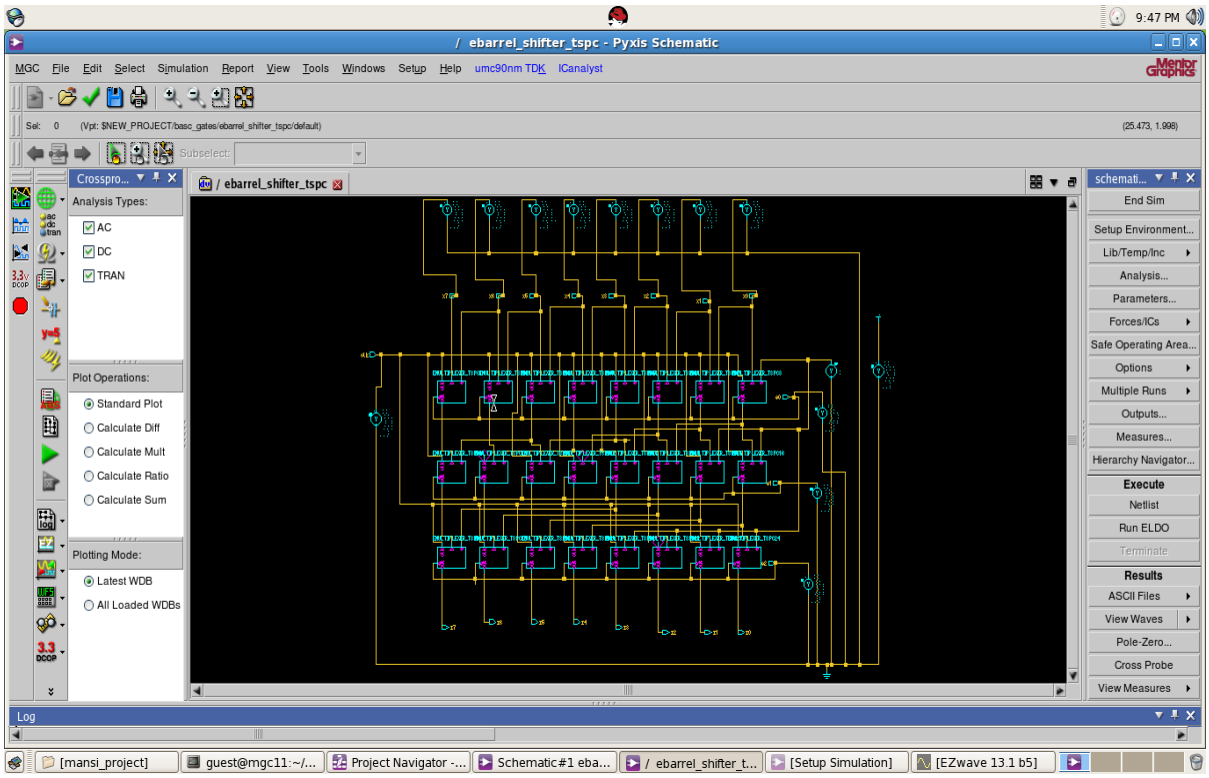


Figure 6: schematic of an 8 bit Left Barrel Shifter

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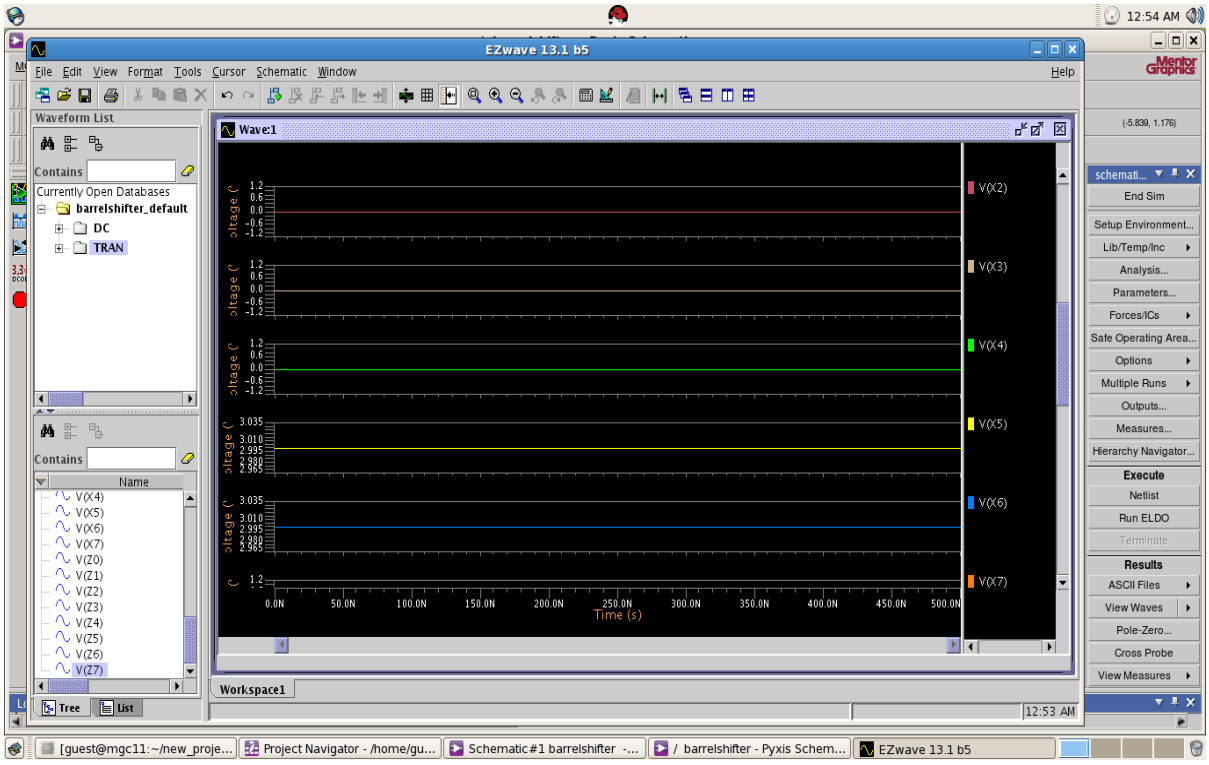
## BARREL SHIFTER OUTPUT WAVEFORM

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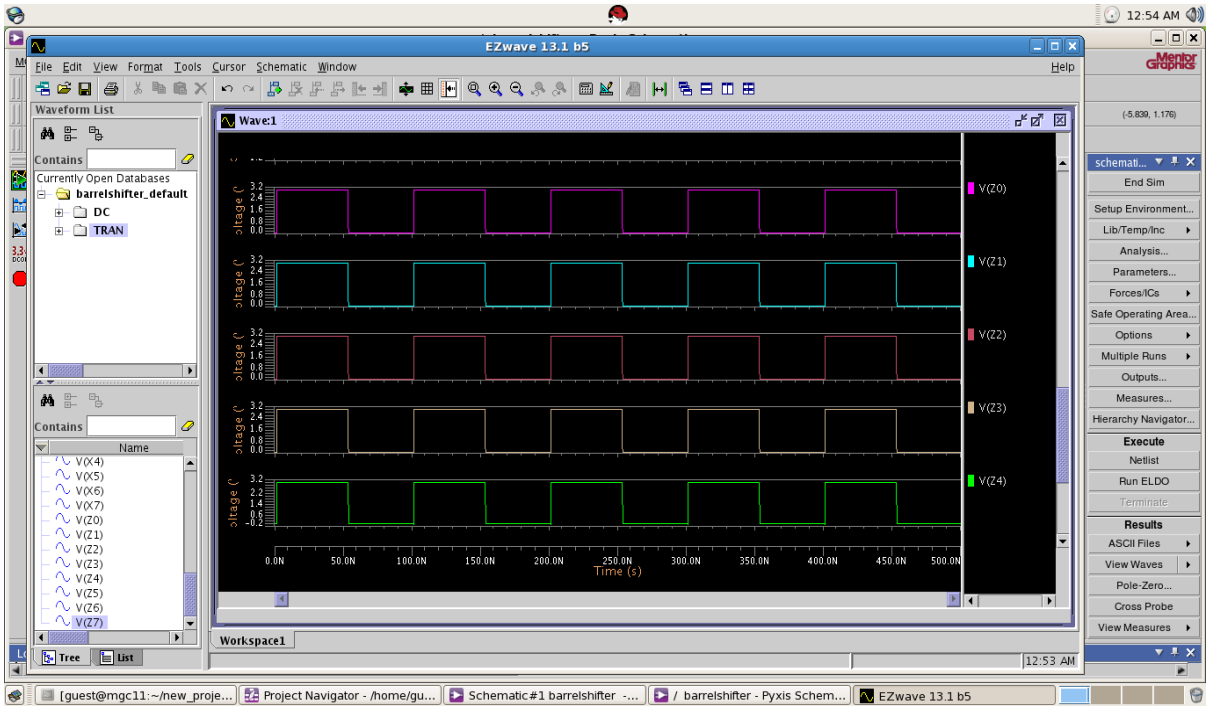


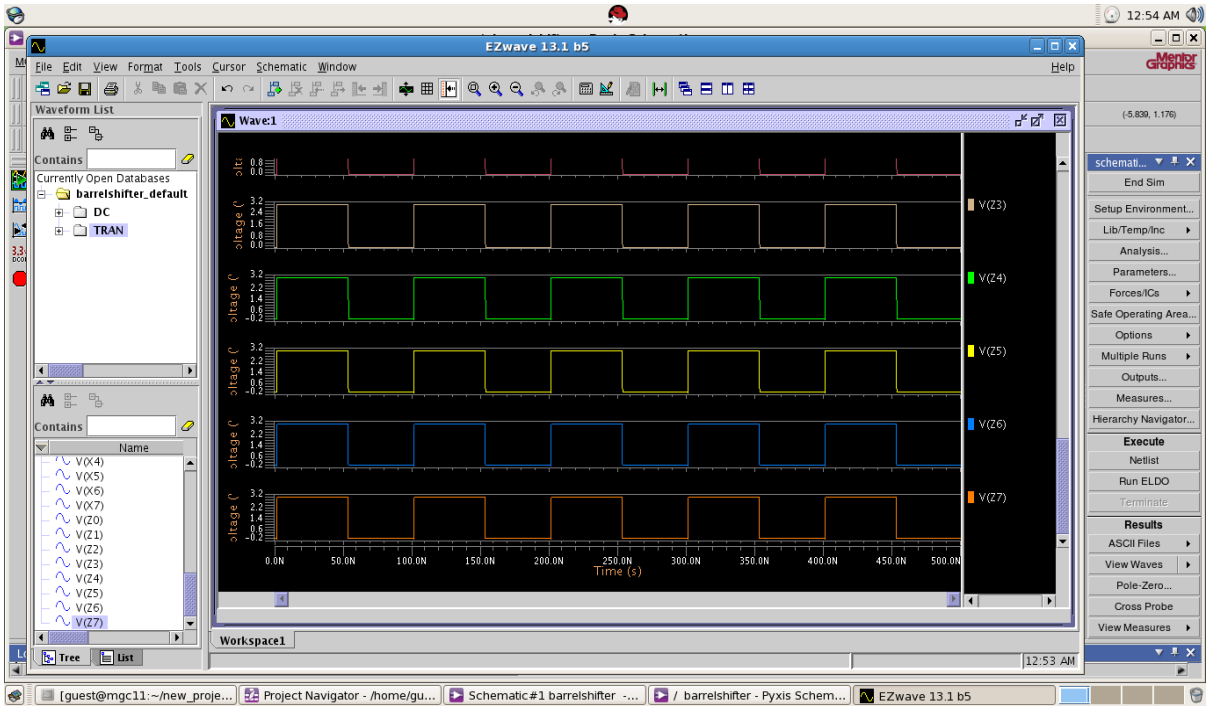


## POWER ANALYSIS

Table 1 summarizes the results of power by 8 bit proposed left barrel shifter incorporating multiplexer circuit. Power consumption of proposed barrel shifter is lower than other shifter designs. This is due to the fact that it combines the advantage of no pre charge pulse propagation by using PDB logic and lower leakage power. The

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power consumed for the TSPC logic based shifter circuit is much larger as compared to PDB dynamic logic based shifter due to higher clock loading.

| | TSPC LOGIC | PDB LOGIC |
|---|---|---|
| MULTIPLEXER | 9.3144 N WATTS | 7.6117 N WATTS |
| BARREL SHIFTER | 9.1756 M WATTS | 7.3944ATTS |

## 5. CONCLUSION

This paper has examined two barrel shifter designs: Tspc based barrel shifter and Pdb based barrel shifter .Power analysis for both the techniques are done and the result is compared. This work can be further extended if we incorporate the SVL logic in the shifter modules for simulation. Measure results and verify that SVL technique based shifter results in lowering the power consumed in ALU.

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