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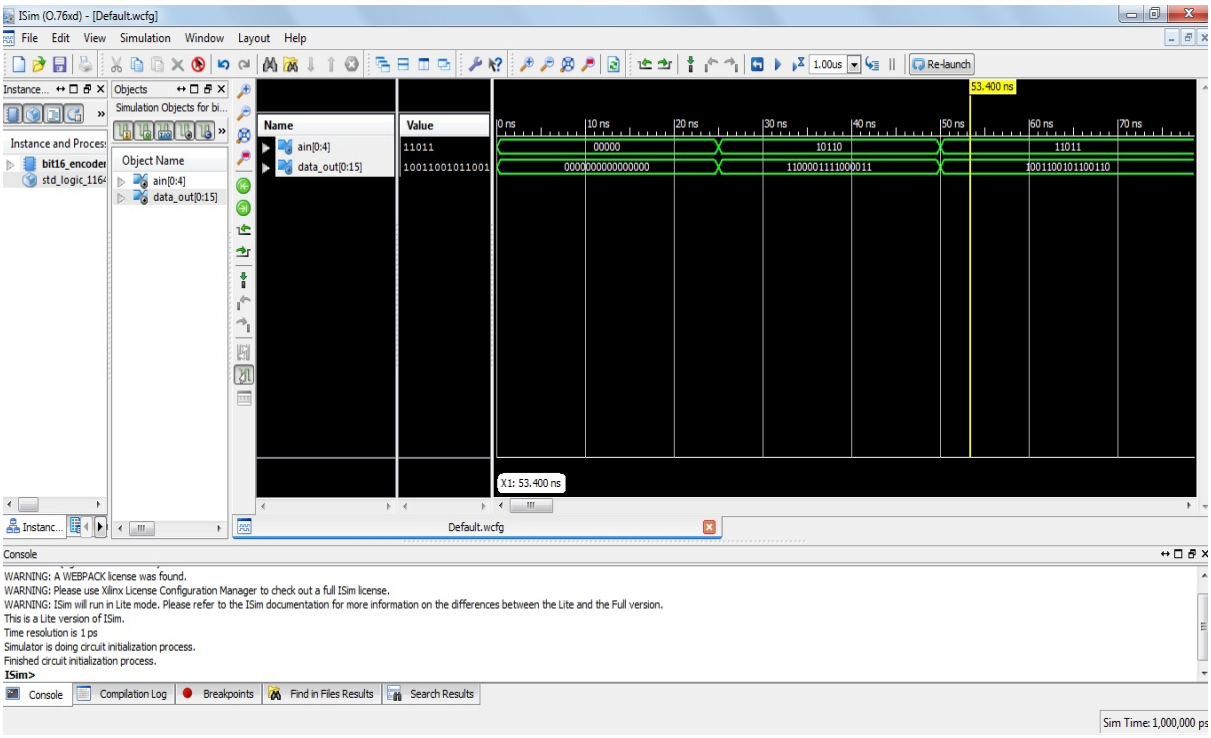
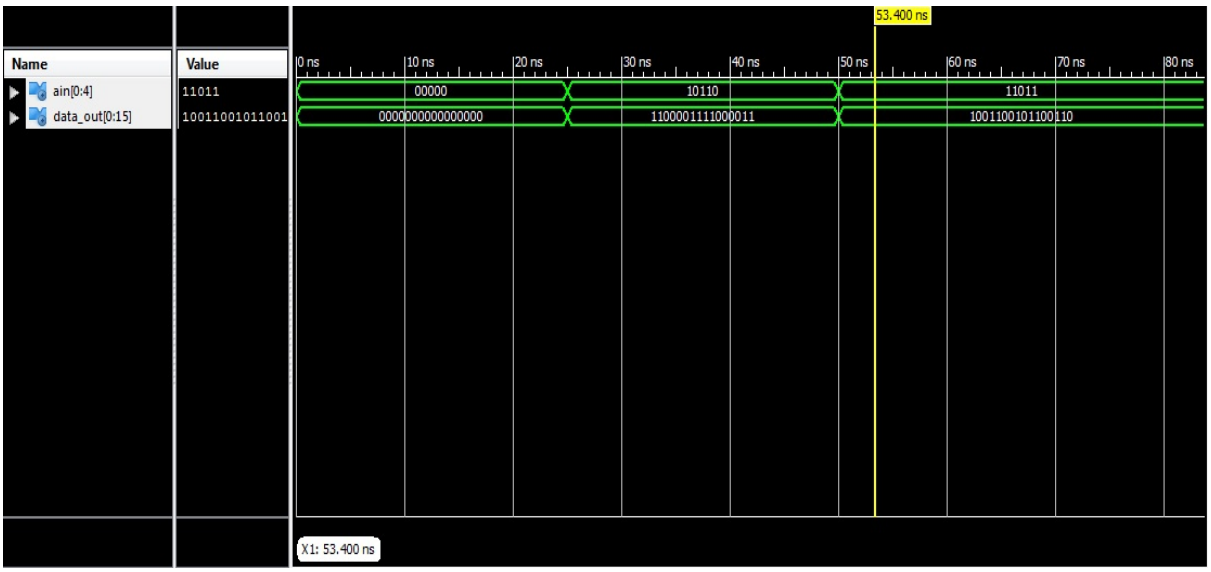
```
                WHEN OTHERS  => DATA_OUT <= "----------------";

END CASE;

        END PROCESS;

END BEHAV;
```

SIMILATION RESULT OF ENCODER





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VHDL CODE FOR RECEIVER

```
LIBRARY IEEE;

USE IEEE.STD_LOGIC_1164.ALL;

ENTITY RECEIVER16 IS

PORT(DIN:IN STD_LOGIC;

                CLK,RST:IN STD_LOGIC;

                AOUT:OUT STD_LOGIC_VECTOR(0 TO 4));

END RECEIVER16;

ARCHITECTURE BEHAV OF RECEIVER16 IS

SIGNAL Z,ZO:STD_LOGIC_VECTOR(0 TO 15);

COMPONENT SIPO16

        PORT(DIN:IN STD_LOGIC;

                CLK,RST:IN STD_LOGIC;

                Z:OUT STD_LOGIC_VECTOR(0 TO 15));

END COMPONENT;

COMPONENT ERRORDET_CORR16

        PORT(Z:IN STD_LOGIC_VECTOR(0 TO 15);

                ZO:OUT STD_LOGIC_VECTOR(0 TO 15));

END COMPONENT;

COMPONENT DECODER16

PORT(ZO:IN STD_LOGIC_VECTOR(0 TO 15);

                AOUT:OUT STD_LOGIC_VECTOR(0 TO 4));
```

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END COMPONENT;

BEGIN

CHIP1:SIPO16

PORT MAP(DIN,CLK,RST,Z);

CHIP2:ERRORDET_CORR16

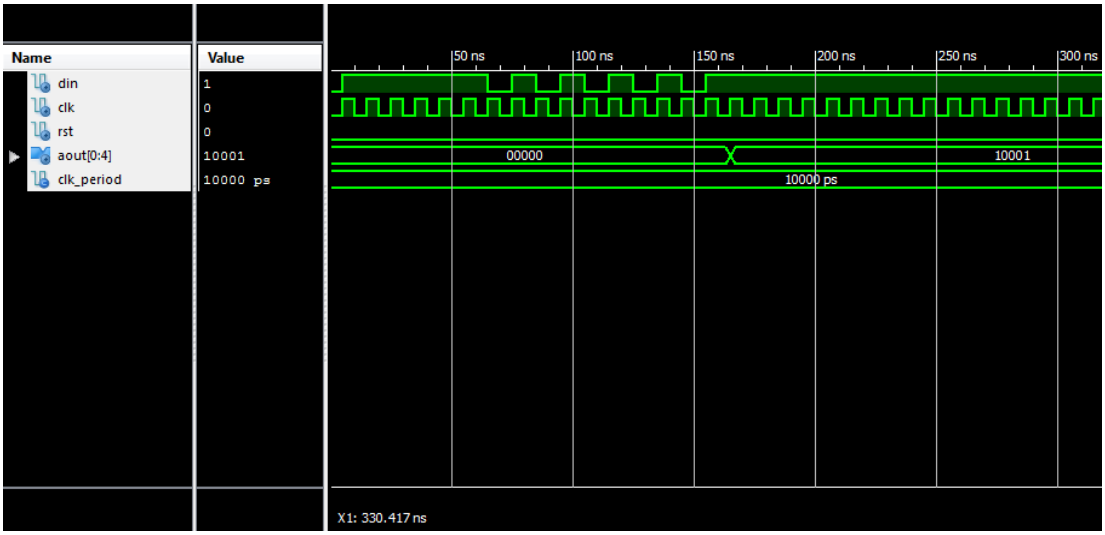
PORT MAP(Z,ZO);

CHIP3:DECODER16

PORT MAP(ZO,AOUT);

END BEHAV;

SIMULATION RESULT OF RECEIVER



VHDL CODE FOR DECODER

LIBRARY IEEE;

USE IEEE.STD_LOGIC_1164.ALL;

ENTITY DECODER16 IS

PORT(ZO:IN STD_LOGIC_VECTOR(0 TO 15);

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```
                AOUT:OUT STD_LOGIC_VECTOR(0 TO 4));
END DECODER16;
ARCHITECTURE BEHAV OF DECODER16 IS
BEGIN
PROCESS(ZO)
        BEGIN
CASE ZO IS
                WHEN "0000000000000000" => AOUT <="00000";
                WHEN "0101010101010101" => AOUT <="00001";
                WHEN "0011001100110011" => AOUT <="00010";
                WHEN "0110011001100110" => AOUT <="00011";
                WHEN "0000111100001111" => AOUT <="00100";
                WHEN "0101101001011010" => AOUT <="00101";
                WHEN "0011110000111100" => AOUT <="00110";
                WHEN "0110100101101001" => AOUT <="00111";
                WHEN "0000000011111111" => AOUT <="01000";
                WHEN "0101010110101010" => AOUT <="01001";
                WHEN "0011001111001100" => AOUT <="01010";
                WHEN "0110011010011001" => AOUT <="01011";
                WHEN "0000111111110000" => AOUT <="01100";
                WHEN "0101101010100101" => AOUT <="01101";
                WHEN "0011110011000011" => AOUT <="01110";
```

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```
WHEN "0110100110010110" => AOUT <="01111";

WHEN "1111111111111111" => AOUT <="10000";

WHEN "1010101010101010" => AOUT <="10001";

WHEN "1100110011001100" => AOUT <="10010";

WHEN "1001100110011001" => AOUT <="10011";

WHEN "1111000011110000" => AOUT <="10100";

WHEN "1010010110100101" => AOUT <="10101";

WHEN "1100001111000011" => AOUT <="10110";

WHEN "1001011010010110" => AOUT <="10111";

 WHEN "1111111100000000" => AOUT <="11000";

WHEN "1010101001010101" => AOUT <="11001";

WHEN "1100110000110011" => AOUT <="11010";

WHEN "1001100101100110" => AOUT <="11011";

WHEN "1111000000001111" => AOUT <="11100";

WHEN "1010010101011010" => AOUT <="11101";

WHEN "1100001100111100" => AOUT <="11110";

WHEN "1001011001101001" => AOUT <="11111";

WHEN OTHERS => AOUT <= "ZZZZZ";

        END CASE;

END PROCESS;

END BEHAV;
```

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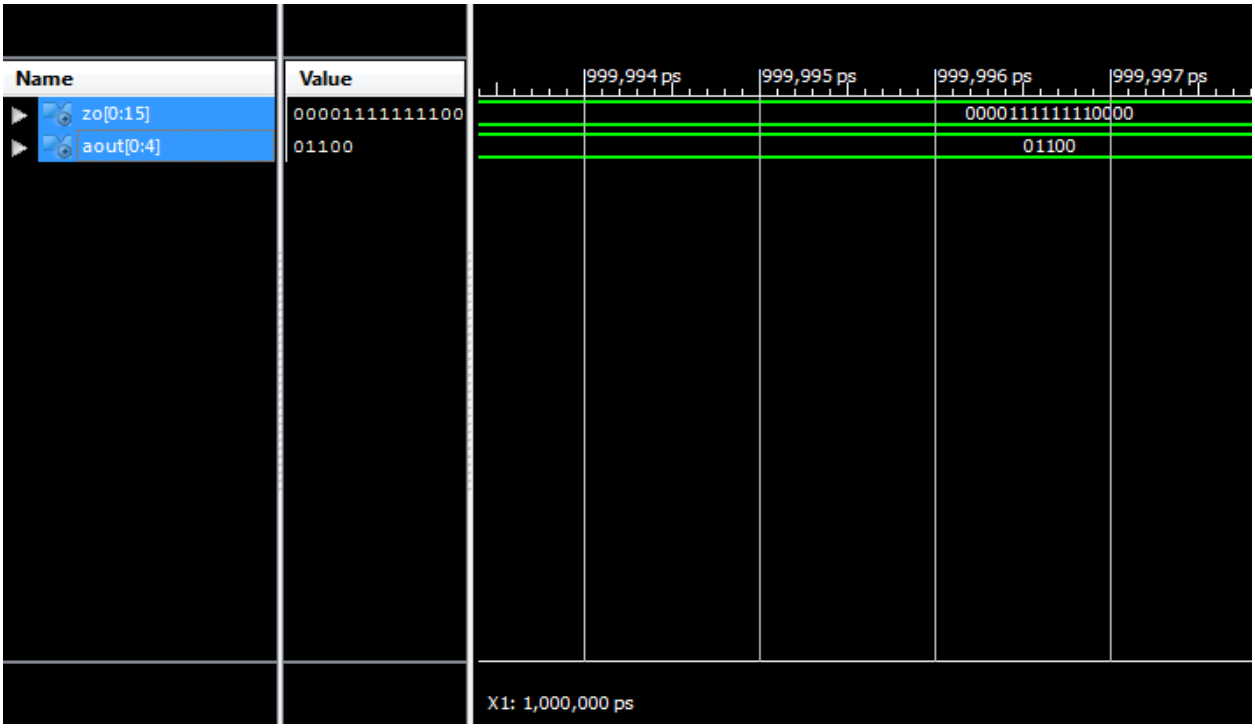
SIMULATION RESULT OF DECODER



5. CONCLUSION

The results of the orthogonal code implementation show that this technique improved the error detection from 50% to93% for 8-bit orthogonal code and 99.9% for 16-bit orthogonal code. The technique proposed can be applied to any encoding system used for digital transmission. Future work includes improvement of correction capasbilities of the orthogonal code and paralell implementation to speed up the data processing.

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