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IMPLEMENTATION OF ZERO-CURRENT-SWITCHING AND ZERO-VOLTAGE-SWITCHING IN INTERLEAVED BOOST CONVERTER

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ABSTRACT

Conventional boost converters that are used are not much sufficient to give soft switching as result switching losses is generated at turn on and off of switches. Due these losses the overall efficiency suffers. To overcome from the problem a new interleveled boost converter by utilizing zero voltage switching (ZVS) and zero current switching (ZCS) is introduced in this work module. It not only reduces input current and output voltage ripple but also it reduces the size and cost of the converter circuit by implementing a common soft switching method. The main achievement of this converter circuit is that a single switch can be used for both ZVS and ZCS characteristic to reduce switching loss and hence efficiency is improved. This converter topology also provides a large variation in load. Operation of this circuit is divided into two areas depending upon the duty cycle of the converter circuit. One operating area has been introduced in this module with its design parameter, theoretically analysis, experimental data and result after simulation is provided in this work module to get the feasible output. Simulation result on varying load is conducted during experiment and the result is provided. Comparison between various types of load on this circuit is also provided for better understanding.

KEYWORDS: *Soft switching, ZVS, ZCS, Boost Converters.*

1. INTRODUCTION

Day by day the rate of increasing electrical power consumption has given rise to the use of power electronics devices to improve the quality of electrical power and for its better controlling. Switch mode power supply (SMPS) has been taken in used due to their ability to withstand across high switching frequency. Another advantage is that they are smaller in size and lighter in weight.

In this work module interleaved boost converter is presented. The topology proposed here is basically a combination of two parallel boost converters with their operating time is 180' apart to each other. In this converter circuit soft switching is implemented among the main and auxiliary switches with characteristic of both Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) during turn ON and turn OFF respectively.

One-off the advantage of this converter circuit is the use of common soft switching technique which reduces the size and cost of converter circuit.

The process of switching in such a way such that the switching transition occurs under favorable condition, i.e. device voltage or current is zero is called as soft switching. In hard switching converters power device used have to be withstand high voltage and high current during turn-on and turn-off process which give a high switching loss and stress across power devices

The converters that consist of combined advantage of PWM converters and resonant converters are called soft switched converters. In soft switched converters resonance is utilized in fully controlled ways which were not done in resonant converters. In this method of switching resonance are asked to occur just before and during turn-on and turn-off time so that the effective ZVS and ZCS can be achieved.

1.1 Zero Voltage Switching (ZVS):

It is one of the techniques which is used to provide soft switching for the power electronics switches. ZVS is used during turn ON of switches in this proposed work module to improve the overall effectiveness of the converter for the broad range of load. ZVS is most widely preferred for switching of MOSFETS for very high switching frequency. In this technique, the voltage across the main and secondary switch are brought to be zero before gate voltage is applied across the switch terminal.

Delay time provided to switch also plays an important role to achieve ZVS condition. For proper achievement of ZVS the delay time must fulfill the criteria below

$$Delay\ time(Td) = \frac{\pi}{2}\sqrt{Leq \times Ce} \qquad (1)$$

1.2 Zero Current Switching (ZCS):

Zero current switching means the current through the switch is prior reduced to zero amperes before switch is being either turn ON or turn OFF. It is another technique which is associated in the process of soft switching of power electronics switches.

ZCS can be achieved during turn OFF by when the switch current is brought to zero before removing the

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gate signal that is being applied during turn ON, means no any flow of carriers in the switch of the converter.

Exclusion of switching losses during turn OFF time and fall in switching losses during turn ON time is seen by applying ZCS in the converter circuit. By implementation of ZCS during turn ON time in resonant converter ideal switching is obtained. However the resonant frequency and that is given by

$$\omega_r = 1/\sqrt{L_r C_r} \qquad (2)$$

Where,

ω_r is the resonant frequency, L_r is the resonant inductance of the resonant converter, C_r is the resonant capacitance of the resonant converter.

2. OPERATIONAL PRINCIPLE

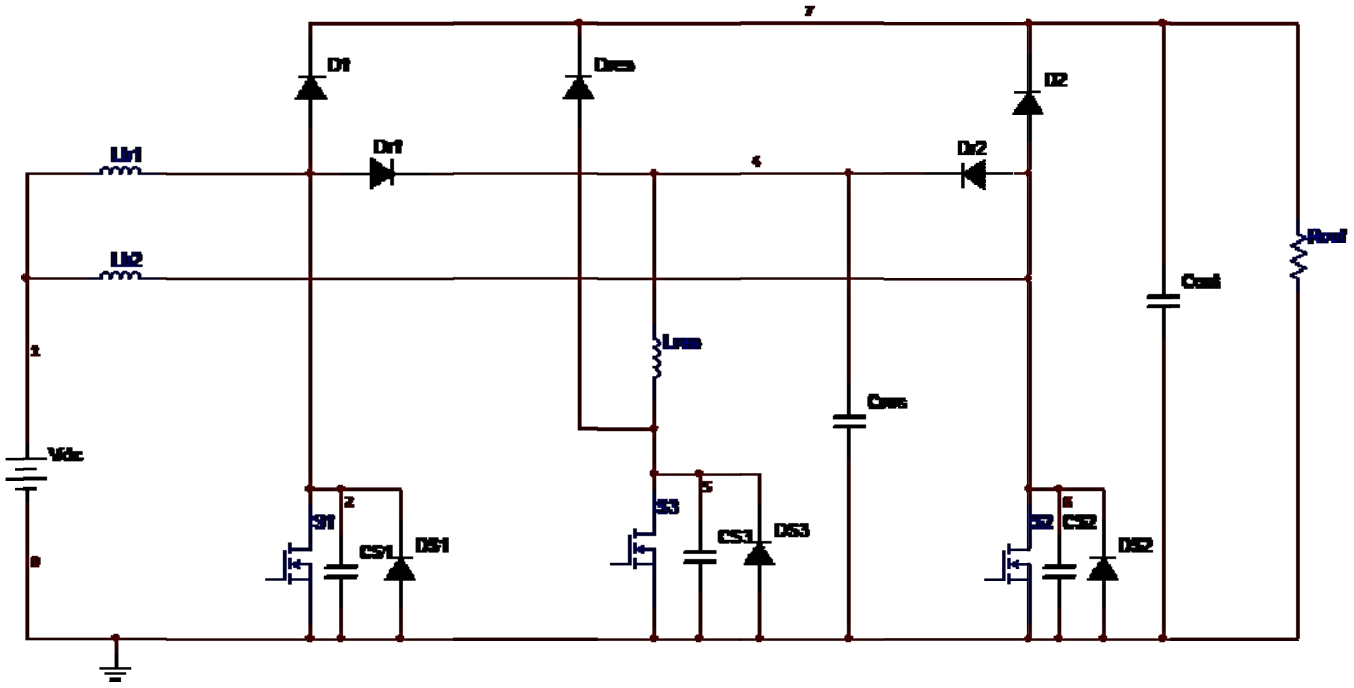

Fig. 2.1. Structural diagram of proposed circuit of interleaved boost converter with having characteristic of both Zero Voltage Switching and Zero Current Switching.

The proposed circuit above is a combination of parallel connected two boost converters, as it is a interleaved topology hence the operation of work is symmetrical. The aim to represent the above circuit is to provide soft switching so that reliable output can be achieved with more increased efficiency. The circuit applies a common soft switching for both parallel connected boost converter which further helps in reducing the size and the overall cost of the topology. The proposed circuit in fig.2.1 shows a resonant circuit which consist of resonant capacitor C_{res}, resonant inductor L_{res} and the parasitic capacitor connected across the parallel of the main MOSFET switches S1 and S2 and the helping switch S3 to provide resonant way to achieve the function of both Zero Voltage Switching and Zero Current Switching. For proper boosting two boost inductor is taken in use namely L_b1 and L_b2.

2.1 Operating Mode:

The operating mode of the circuit is classified into two types depending upon the duty cycle of the main power electronic switches connected in the topology

The two operating mode of the proposed circuit is divided on the behalf of duty cycle (**D**). The duty cycle of this converter is given by:

$$D = (V_{out} - V_{in})/V_{out} \qquad (3)$$

Where, D = Duty Cycle of the converter, V_{in} = Input Voltage supplied, V_{out} = Converter output voltage.

In this work module we have focus light only on the one mode of operation which is being discussed below. However the circuit topology will remain same but the switching timing of power electronics switches will be changed during both mode.

2.2 Operational Analysis of Proposed Topology (when Duty cycle is less than 50%):

The principle of operation of the above presented circuit topology of boost converter with duty cycle D less than 50% is illustrated in this section of work module.

Before going on operational analysis it is to be noted for some assumption taken during the operation. These assumptions are:

1. The power electronics switches and the diode taken in use are ideal.
2. The Boost inductors namely L_b1 and L_b2 are equal. ($L_b1 = L_b2$).
3. Main switches pose same duty cycle. (D1 = D2).
4. The output capacitor used is ideal in nature.

By the switching configuration there are 14 modes of operation in this topology according to switching timing. As the converter is of interleaved hence only seven modes is discussed and the other seven modes are

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symmetrical to previous seven modes. The switching modes that illustrated in this section are from MODE A to MODE G.

MODE A [t_a – t_b]: The circuit represented in fig. 2.1. is the proposed circuit for the operation. In this operating mode all the main switches S1 and S2 and the helping switch S3 are in conducting state. However the power diodes D1, D2 and the resonant diode D_r are reversed biased and behaves as in position off. The current through the main switches are less than zero or it may be equal to zero when the prior mode ends.

In this mode the Zero Voltage Switching is achieved by the main switch S2 when this ends at time t = t_b.

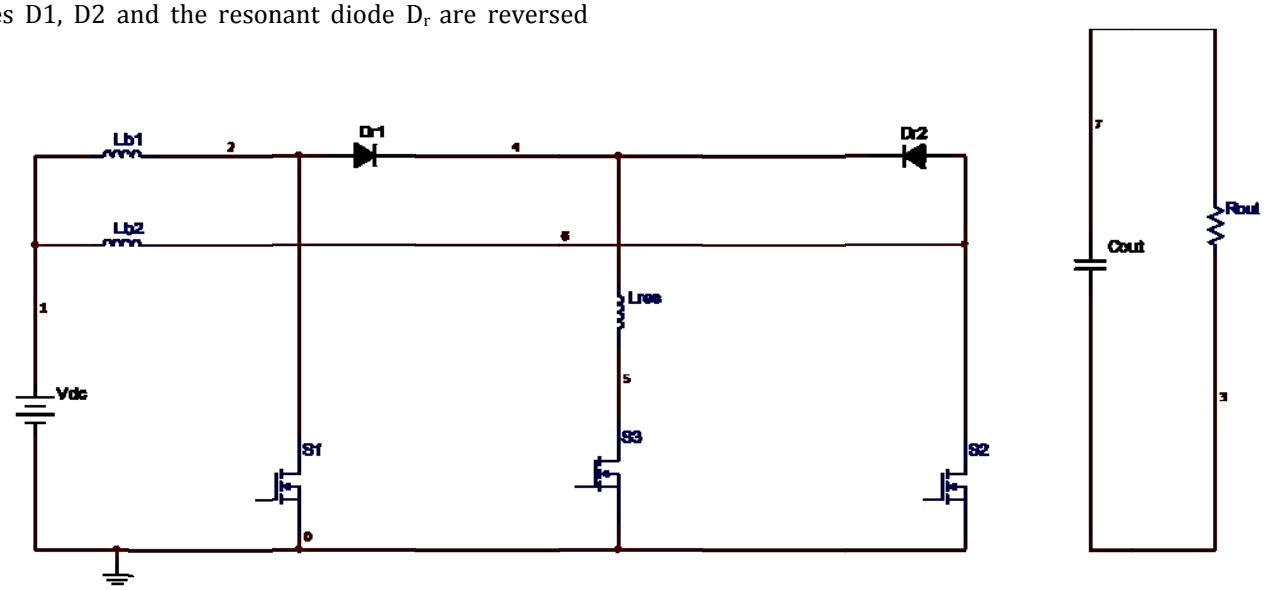

Fig. 2.4. Equivalent circuit of the proposed converter topology in the operating mode A.

The time interval of this mode is given by t_{ab} and that is:

$t_{ab} = (D1 - 0.5)\ T$ (4)

Where,

T = Total time period of the switch.

$T = T_{on} + T_{off.}$ (5)

MODE B [t_b t_c]: Resonant inductor connected in series with the helping switch in the topology plays a very important role in this mode of operation. In this mode the energy stored in that inductor namely L_r is transferred to the load connected at the output of the converter section through the power diode D_r. This happens due to the present off condition of the helping switch in this mode. At time t_c the diode connected with the resonant inductor will turn off due to linearly decrement in the resonant inductor current.

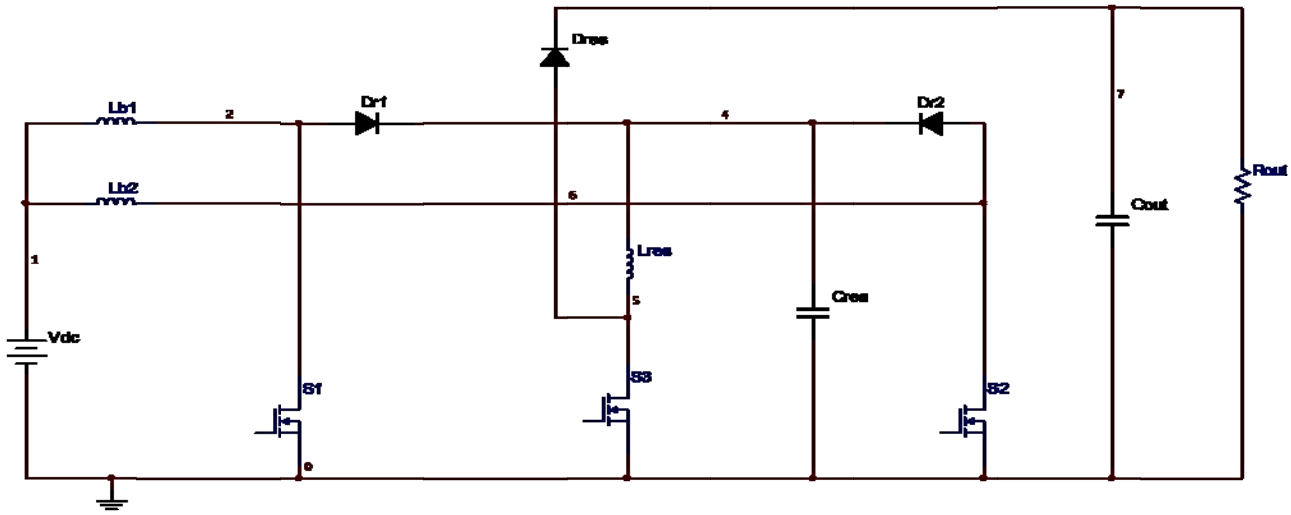

Fig. 2.5. Equivalent circuit of the proposed converter topology for operating mode B

The time period of this mode is given by 't_{bc}':

$t_{bc} = (L_r / V_o) * I_{in}$ (6)

Where,

V_o = output voltage of the converter circuit, I_{in} = Input current

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MODE C [t_c – t_d] : At the starting of this mode the diode connected with the resonant inductor is turned off and the energy stored in the second boost inductor (L_{b2}) and the parasitic capacitor (C_{s2}) of the helping switch S_2 is transferred to the resonant inductor, resonant capacitor and the parasitic capacitor of the second main switch S_2 of the circuit. In this mode the power diode D_2 will turn on when the voltage across the main switch S_2 and the voltage across the resonant capacitor will reach to the output voltage V_o.

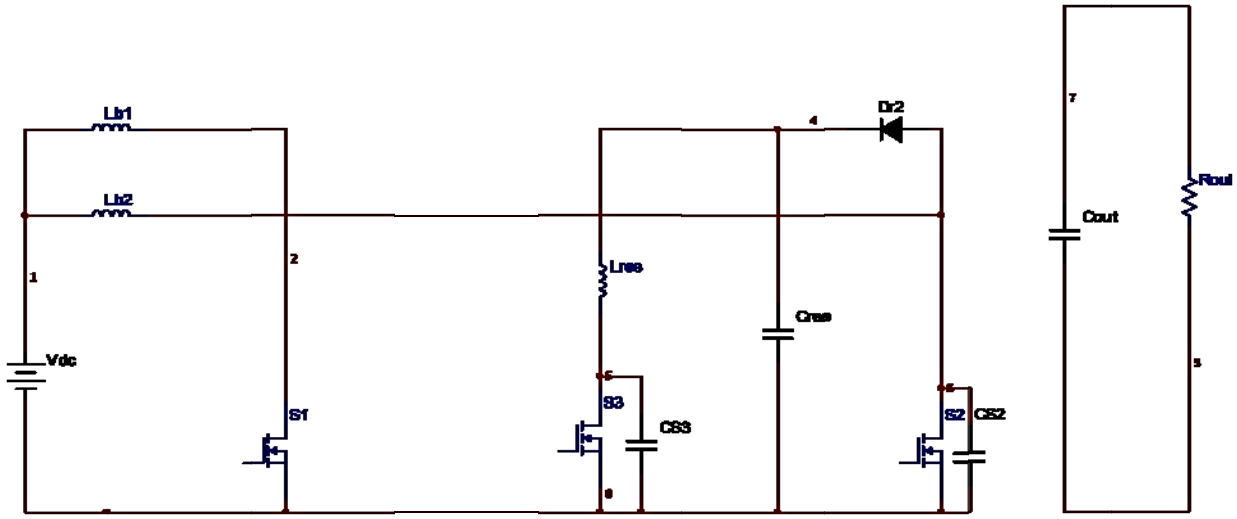

Fig. 2.6. Equivalent circuit of the proposed converter topology for operating mode C.

The time interval in this mode is given by "t_{cd}" and that is:

$$T_{cd} = \pi \sqrt{(L_r * C * C_{s2}) / (C + C_{s2})} \quad (7)$$

Where,

C_{s2} is the parasitic capacitor connected across the main switch S_2.

C is the equivalent capacitance which is given as

$$C = C_r + C_{s2} \quad (8)$$

MODE D [t_d - t_e] : In this mode the parasitic capacitor C_{s3} connected across the helping switch is gradually charged to the value of output voltage. After that the power diode D_r connected with the resonant inductor is seen to be turn on at the time t_e.

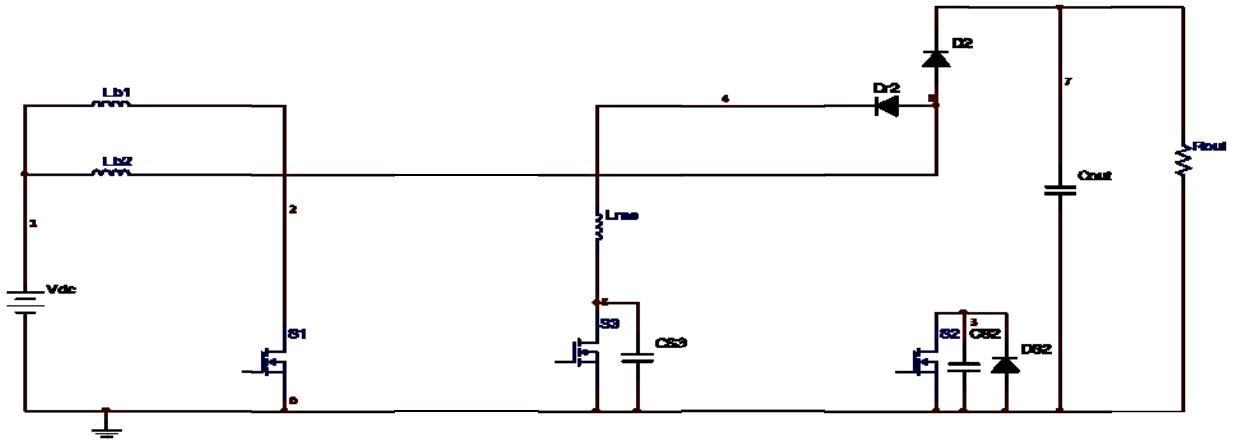

Fig. 2.7. Equivalent circuit of the proposed converter topology for operating mode D.

The time interval of this mode is given by " t_{de} " which is:

$$T_{de} = (C_{s2} * V_o) / (I_{LB2} - I_o) \quad (9)$$

Where, I_{LB2} is the current through the boost inductor 2.

MODE E [t_e - t_f] : when the previous mode ends at time t_e the power diode D_r is turned on. In this mode the energy stored in the resonant inductor is transferred to the load connected to the output of the converter topology by the power diode D_r. The process will continue till the helping switch S_2 is not triggered ON. The switch S_2 will be switched ON at time t = t_f and at time the power diode D_r will turned off.

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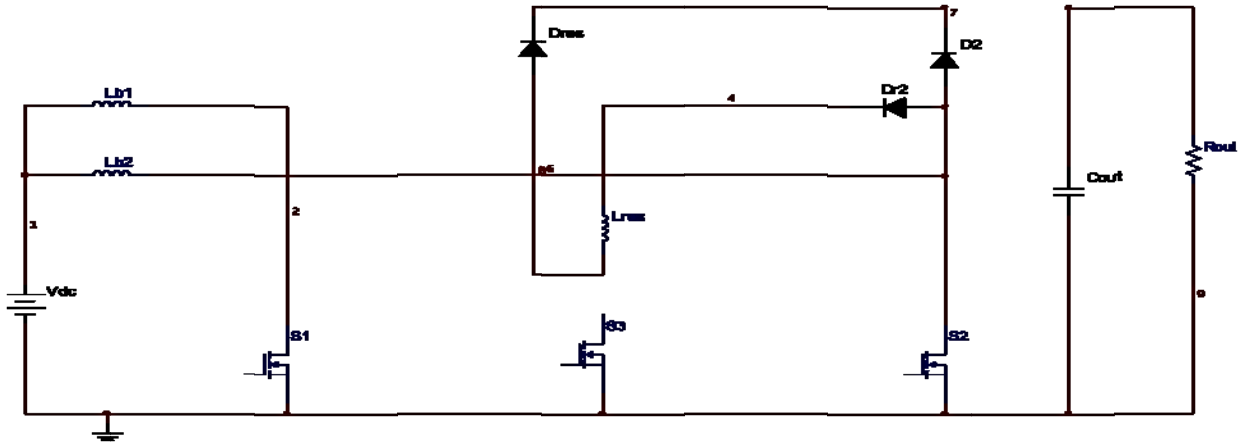

Fig. 2.8. Equivalent circuit of the proposed converter topology for operating mode E.

The time interval of this mode is given by " t_{ef}" which is:

$$t_{ef} = 0.5\ T - t_{ae} - D_k T \quad (10)$$

Where,

t_{ae} is the time interval between the time of t_a to t_e.

And,

D_kT is the time period at which the helping switch is conducting with main switch S_1 also conducting but at this time period the switch S_2 will be in off condition.

The resonant inductor current in this mode is taken as:

$$I_{Lr}(t_f) = I_{Lr}(t_e) \quad (11)$$

MODE F [t_f - t_g] : In this mode the working period is divided into two parts. One is from [t_f – t_1] and another is from [t_1 - t_g]. In the time interval of [t_f – t_1] the current in the resonant inductor gradually increases till it achieve the value of the boost inductor (L_{b2}) current. The current through the power diode D_2 is I_{D2} which gradually decreases to zero at time reaches to value of t_1.

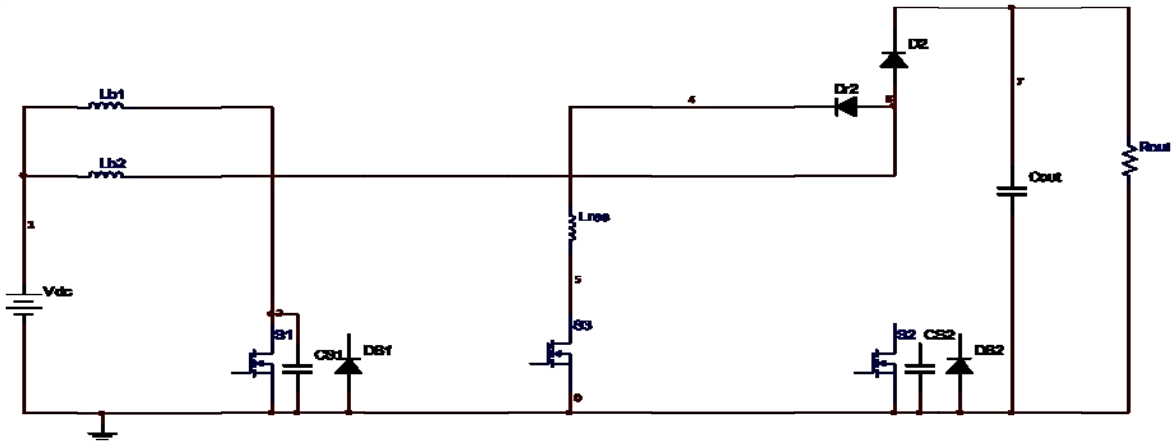

Fig. 2.9. Equivalent circuit of the proposed converter topology for operating mode F.

The time interval of this working period is given by " t_{f1}" and that is:

$$t_{f1} = L_r * (I_o / V_o) \quad (12)$$

For the time interval [t_1 - t_g] the current through the resonant inductor persist to increase to attain the peak value and the voltage across the main switch S_2 decreases to zero due to the effect of resonance among C_{s2}, L_r and C_r.

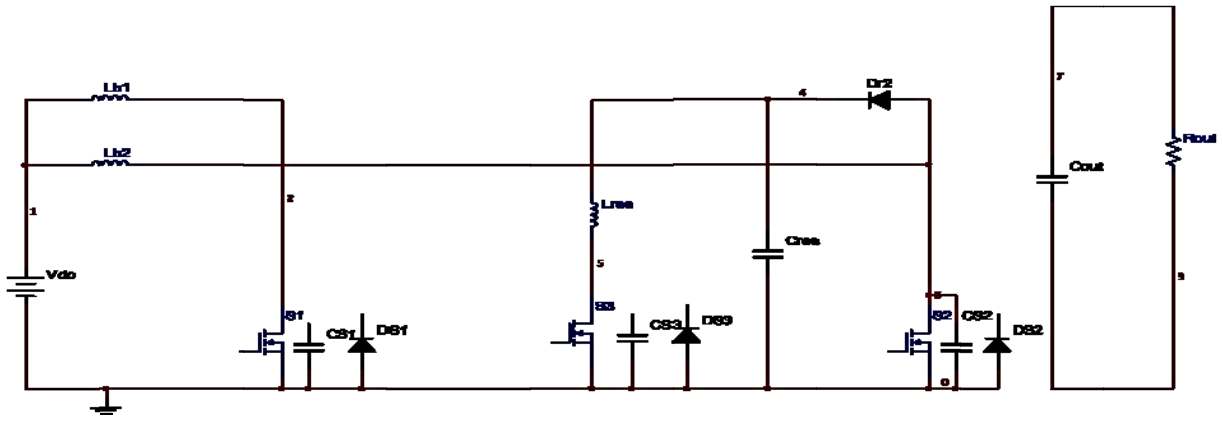

Fig. 2.10. Equivalent circuit of the proposed converter topology for operating mode F.

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At time t_g the diode D_{S2} connected across the main switch S_2 is switched on.

The time interval of this working period is given by "t_{1g}" which is:

$$t_{1g} = \pi / 2\omega_1 = (\pi / 2) (\sqrt{L_r} * (C_{S2} + C_r)) \quad (13)$$

And the total time interval of this mode is given by "t_{fg}" and that is:

$$T_{fg} = L_r * (I_o / V_o) + (\pi / 2) (\sqrt{L_r} * (C_{S2} + C_r)) \quad (14)$$

MODE G [t_g - t_h] : This mode starts when the voltage across the main switch S_2 and the voltage across the resonant capacitor equals to zero and the power diode connected across the switch S_2 is turned on. In this mode to achieve ZCS condition the main switch S_1 can be turned off. The main switch S_2 pose ZVS characteristic in this mode due to the diode D_{S2} connected across it.

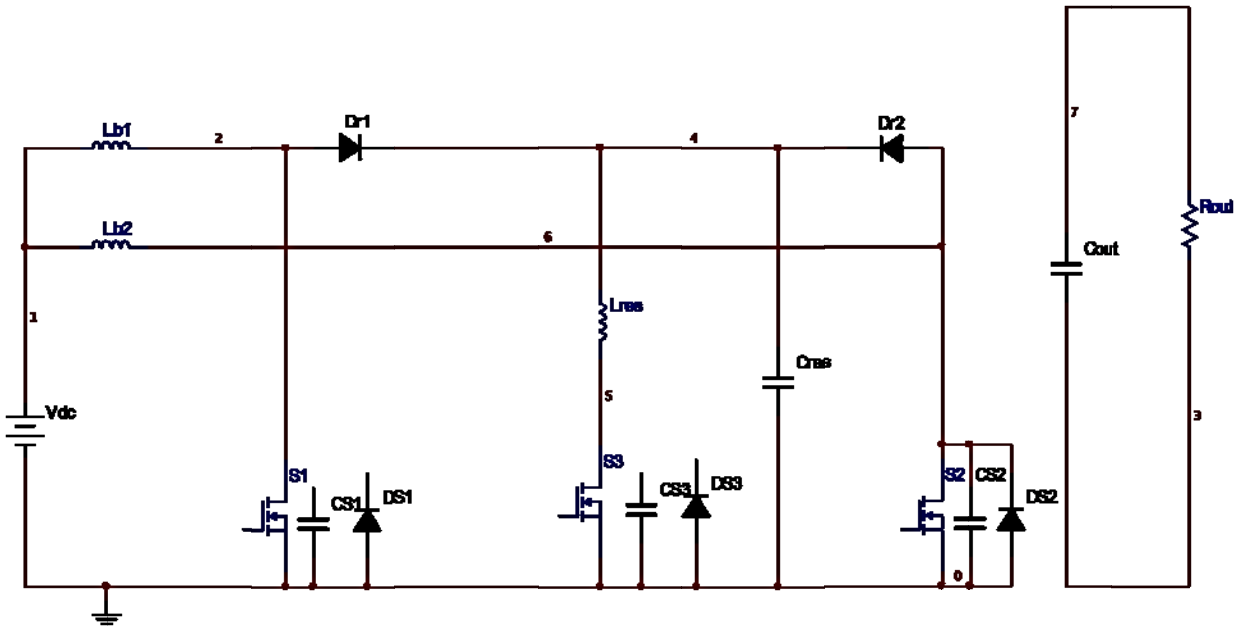

Fig. 2.11. Equivalent circuit of the proposed converter topology for operating mode G.

The time interval of this mode is given by "t_{gh}" and that is:

$$T_{gh} = 0.5\ T - t_{ag} \quad (15)$$

Where,

T_{ag} is the time period between time t_a and t_b.

2.3 Voltage conversion:

As the proposed topology is boost topology the output voltage we achieve by this converter is larger than the input is supplied, however the proposed circuit not only provides higher output voltage but also soft switching increases the conversion rate.

$$\text{Voltage conversion} = (V_o / V_{in}) \quad (16)$$

$$V_o / V_{in} = 1 / (1 - (D_1 + D_k)) \quad (17)$$

Where,

D_1 is the duty cycle of main switch S_1.

And,

D_k is the duty cycle of switch S_3 when S_2 is off and S_1 is on.

3. SIMULATION AND ITS RESULT

In this work module the simulation of proposed circuit topology is done through the MATLAB™ of version R2009b.

3.1 Simulation by MATLAB™.

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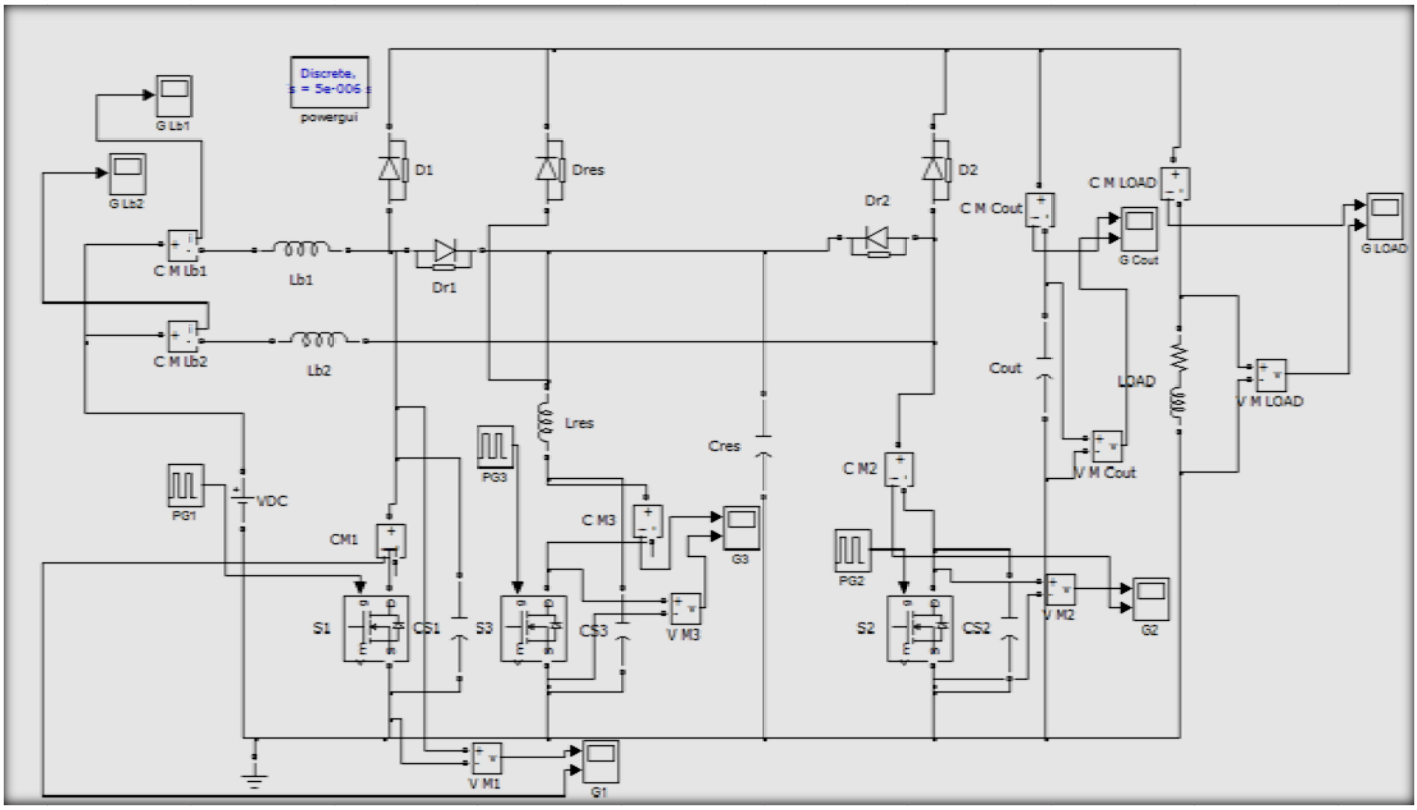

Fig. 4.1. Equivalent circuit of proposed topology in SIMULINK.

Table 4.1. Components and their parameter for simulate the proposed circuit

SYMBOL	PARAMETER	SPECIFICATION
Input Voltage	V_{dc}	120V to 250V
Output Voltage	V_o	390V
Duty Cycle	D	D< 50%
Switching Frequency	f_s	50 kHz
Boost Inductors	L_{b1} , L_{b2}	2.4 mH
Resonant Inductor	L_{res}	10 µH
Resonant Capacitor	C_{res}	1.5 nF
Main Switches	S_1 , S_2	IRF840
Helping Switch	S_3	IRFP460
Power Diode	D_1 , D_2	HFA08TB60
Helping Diode	D_{res} , D_{r1} , D_{r2}	HFA08TB60
Output Current	I_o	0.4A to 1.0 A
Output Capacitor	C_{out}	470 µF
Output Power	P_{out}	150 to 300 W

Load Current and Voltage:

The output of the converter is connected with the RL load. When the dc source is applied then the graph below is obtained as the voltage and current characteristic of Load.

Load Current:

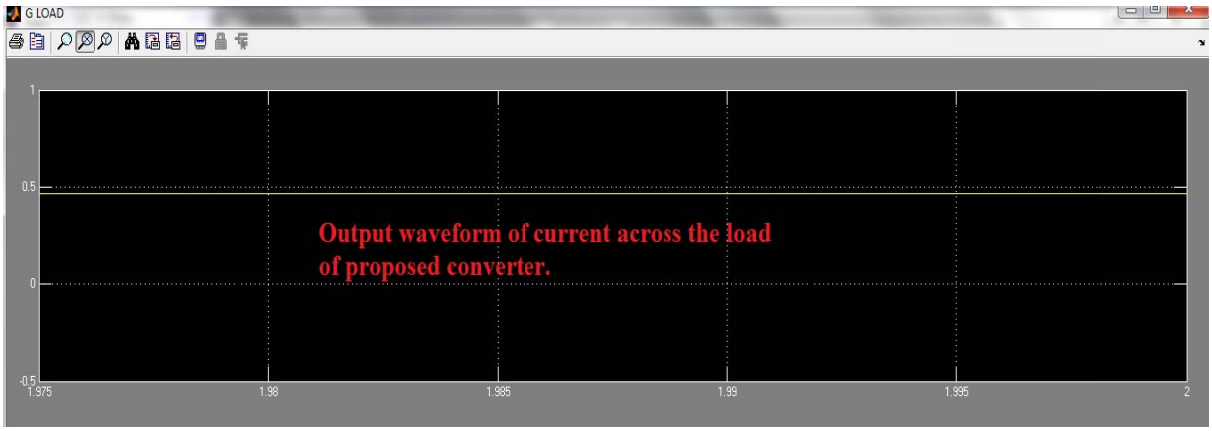

Fig. 4.2. Current through the load

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In the above figure the load current is achieved is approximate value of 0.468 A while the input voltage feed to the circuit is V dc of value 190 V. It is clear that the output we achieve is free from ripple which denotes the effectiveness of the circuit used in this topology. Due to the use of high value of resistance the current is in limited order and is under excepted value which ranges from 0.4A to 1.0 A

Load Voltage:

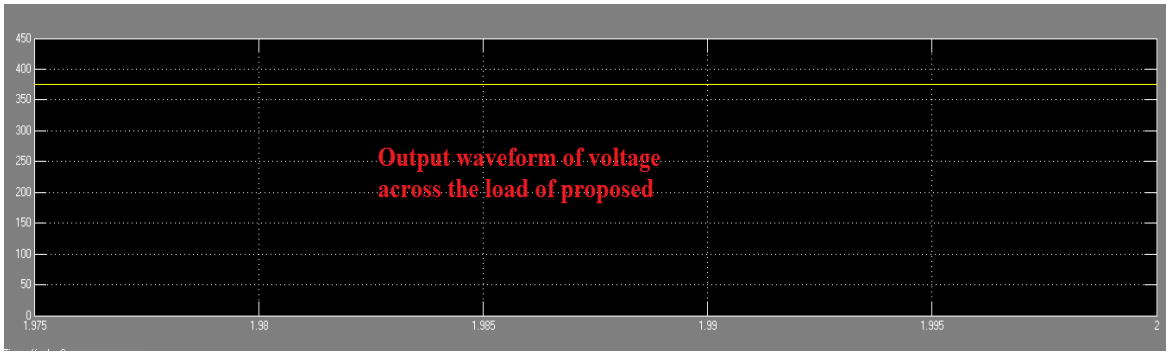

Fig. 4.3. Voltage across the load

The above figure shows the output voltage characteristic of load connected across the output of the proposed converter topology.

This voltage waveform of load is achieved when the supply to the converter circuit is feed at 190 V dc. The load connected at the output is RL type in which the resistance of load is about 800Ω and inductance about 500mH. The load voltage achieved through the conversion is about 376V which satisfy the duty cycle ratio of the converter topology. Absence of ripple in the output gives raise the effectiveness of the topology which can be treated as better result of conversion.

From equation (3);

$D = (V_{out} - V_{in}) / V_{out}$

$D = (376 - 190) / 376$

$D = 0.49 = 49\% < 50\%$ (28)

Equation (28) satisfy the mode of operation of proposed circuit topology presented in this work module, the duty cycle ratio from the equation states that the analysis done in the work module and all the assumption that has been taken is totally right.

On the other hand the voltage conversion ratio for this proposed topology is given by equation (16) and (17).

From equation (16) and (17);

Voltage conversion = (V_o / V_{in})

$= 376 / 190$

$V_o / V_{in} = 1 / (1 - (D_1 + D_k)) = 376 / 190$

≈ 1.98 (29)

Equation (29) shows the voltage conversion ratio of the proposed topology which is also satisfied by the equation derived earlier in this work module.

The above two figure shows the output current and voltage waveform of the converter circuit which feed the output power to the load. All the result discussed above is totally right and simulated correctly to achieve proper accuracy.

After getting the behaviour of load current and voltage the simulation parameter will now focus on the behaviour of switches during simulation of this work module. For switches soft switching is implemented that's why next section is fully dedicated to the switching behaviour of switches.

Switching characteristic of switch S_1.

When the input dc voltage source is applied then it reaches to switch S_1 via the boost inductor L_{b1}. The input that the switch is feed is with pulse generator with switching frequency of 50kHz and the input voltage through the dc source of 190 V.

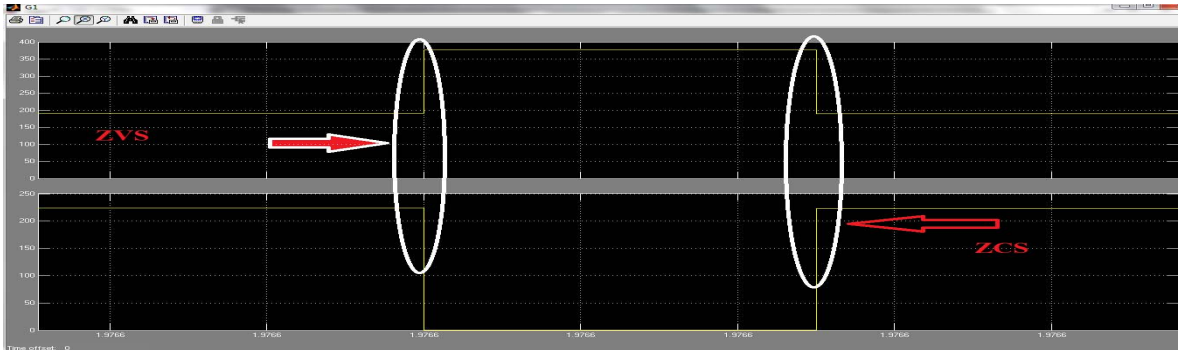

Fig. 4.4. Switching characteristics of S_1 with voltage at top

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Above figure shown is the switching characteristic of main switch S_1. In the above graph the position of ZVS and ZCS is shown. The ZVS is achieved for switching on the switch while ZCS is achieved when switch is going to be off.

Before ZVS condition the voltage across the switch is brought to minimum value and that time the value of current across the switch is maximum. The above graph where voltage and current waveform is plotted with respect to time shows the current is in Zero state when the voltage is in maximum across the switch.

During ZCS condition the switch voltage is maximum and the current is minimum and hence the characteristic is achieved switching off the switch.

Switching characteristic of switch S_2.

When the input dc voltage source is applied then it reaches to switch S_2 via the boost inductor $L_{b2.}$ The input that the switch is feed is with pulse generator with switching frequency of 50 kHz and the input voltage through the dc source of 190 V. However the change in the switching frequency can be done for the fulfilment of demand.

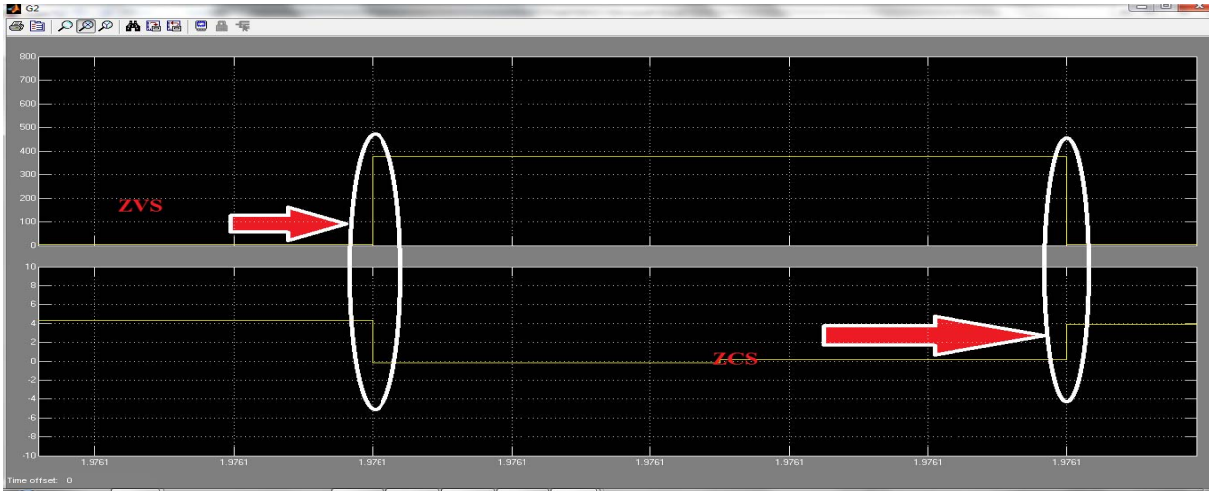

Fig. 4.5 Switching characteristics of $S_{2.}$with current at below.

The above figure shown is the switching characteristic one of the main switches, S_2. In the above graph the position of ZVS and ZCS is shown. The ZVS is achieved for switching on the switch while ZCS is achieved when switch is going to be off.

The above graph where voltage and current waveform is plotted with respect to time shows the current is in Zero state when the voltage is in maximum across the switch. Before ZVS condition the voltage across the switch is brought to minimum value and that time the value of current across the switch is seen to be maximum.

In the above figure it can be easily illustrated that during ZCS condition the switch voltage is maximum while the current is minimum and hence the ZCS characteristic is achieved during switching off the switch.

Switching characteristic of switch S_3.

When the input dc voltage source is applied then it reaches to switch S_3 via the boost inductor $L_{b1.}$ The input that the switch is feed is with pulse generator with switching frequency of 50kHz and the input voltage through the dc source of 190 V. More ever the switching frequency are taken almost double for the helping switch.

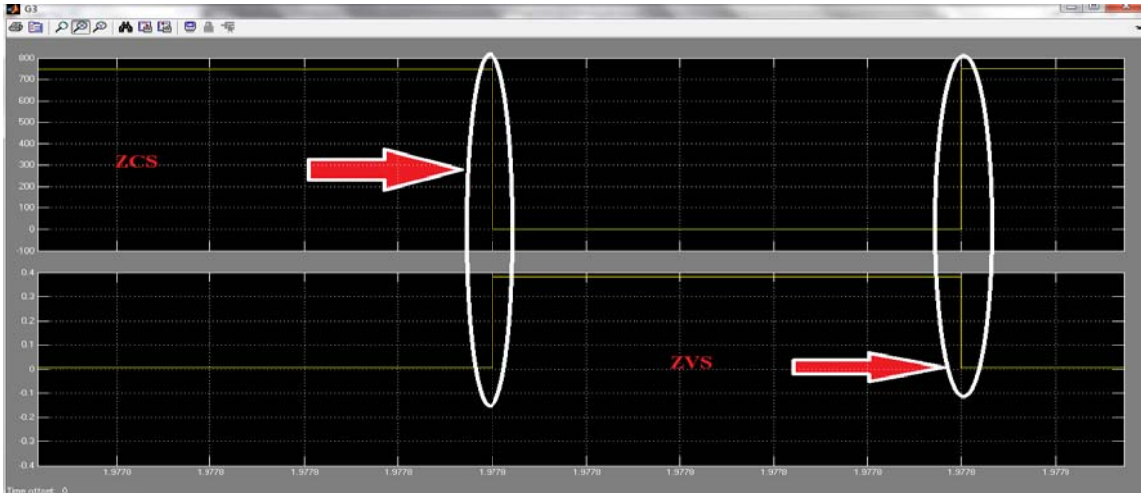

Fig. 4.6 Switching characteristics of $S_{3.}$with voltage at top.

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The above figure shown is the switching characteristic one of the helping or auxiliary switch, S_3. In the above graph the position of ZVS and ZCS is shown. The ZVS is achieved for switching on the switch while ZCS is achieved when switch is going to be off.

Due to the high voltage stress present on the switch S_3 the configuration of the switch is different than the main switches. Before ZVS condition the voltage across the switch is brought to minimum value and that time the value of current across the switch is seen to be maximum.

In the above figure it can be illustrated easily that during ZCS condition the switch current is minimum and the voltage across the switch is maximum and hence the ZCS characteristic is achieved during switching off the switch.

Characteristic of output Capacitor.

The output capacitor is connected across the output of the converter circuit of the proposed topology. It is placed parallel to the load which somehow used as filter capacitor to reduce the harmonics in the output.

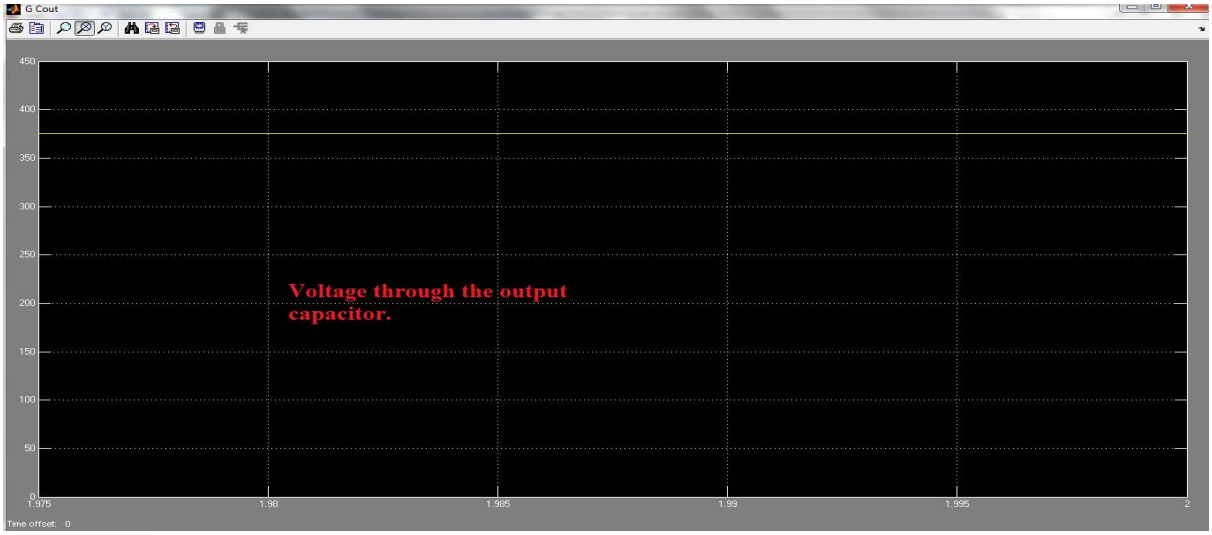

Fig. 4.7 Voltage characteristics of output capacitor (C_{out})

The voltage across the output capacitor is noted same as that of the load. Capacitance of output capacitor is of 470μF and the voltage across the capacitor is 376 V. The waveform achieved is symmetrical to the voltage waveform of the load.

Power Output

The output power of the converter circuit for a particular load is given by:

$$P_{out} = V_{out} * I_{out} \quad (30)$$

Where,

V_{out} = Output Voltage.

I_{out} = Output Current.

The load connected across the output terminal of load is RL type having resistance of 800Ω and inductance of 500mH.

Then from equation (30);

$P_{out} = 376 * 0.47$

= 177 watt.

The power output is in expected range and hence satisfy the operation of converter circuit.

4. CONCLUSION

In this work module the interleaved boost converter topology has been presented. The proposed topology can work on both modes of operation. However the load characteristic and the voltage conversion of the converter have been discussed which shows that the converter fulfils the requirement that is needed.

The soft switching is achieved successfully for main switches and the presence of resonant inductor and resonant capacitor along with auxiliary switch with parasitic capacitor provides resonant way to achieve ZVS and ZCS condition.

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