Leakage Power Optimization by Sleepy Keeper Gate Replacement Techniques

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Abstract

Power dissipation becoming a limiting factor in VLSI circuits and systems. Due to relatively high complexity of VLSI systems used in various applications, the power dissipation in CMOS inverter arises from its switching activity, which is mainly influenced by the supply voltage and effective capacitance. One of challenge with technology scaling is the rapid increase in sub threshold leakage power due to Vt reduction. Leakage power dissipation is a component of static power dissipation in CMOS circuits. It is caused by the presence of leakage currents in the MOS transistors. Leakage power can be reduce by Stack, Sleep and Sleepy keeper transistor techniques. Sleepy Keeper technique provided lesser static power dissipation and lesser static power delay product in comparison with the other techniques. The main advantage of using Sleepy Keeper technique is that it retains the logic state and also lowers the sub threshold leakage power dissipation. It has been shown previously that the stacking of two off transistors has significantly reduced sub-threshold leakage compared to a single off transistor.