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VHDL MODEL OF SMART SENSOR

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ABSTRACT

The paper focus on VHDL model of smart sensor is proposed to obtain solution to the challenge of designers. It is an optimal platform for implementing algorithm for smart sensor unit for noise reduction (noise cancellation of voice signal) using IEEE 1451 standard. There are lots of researches on noise cancellation but using smart sensor for sensing real time voice with the interfered noise will be more efficient. To achieve good result the signal is first sensed using signal sensing process then it is conditioned & processed using VHDL. The VHDL program we have developed acts as the smart sensor as above mentioned step. The VHDL allows the complete simulation of entire system & hence it is possible to simulate together parameter of different domain.

KEY WORDS: IEEE1451, smart sensor, VHDL

1. INTRODUCTION

An evolving semiconductor technology has resulted in the low cost microprocessor, hence the design & overall cost of the control system can be minimized as it is built on single chip. The idea of incorporating the electronics & the sensor is to develop the intelligent sensor. Smart sensors are extremely growing & are used across all over the industries. Growing demand of smart sensor & field network technologies have led the networking of smart sensor a very economical & attractive solution for broad range of measurement & control application. The main aim of smart sensor in an integrating electronics is to perform logic function, two way communications& making the decision. Smart sensors are capable to provide desired output & interpretive power which constantly improves smart sensor performance & capabilities. So recently the on growing adoption &

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

importance of smart sensor for real time application has increased rapidly & manufactures are constantly taking efforts in developing the efficient & effective smart sensor.

2. SMART SENSORS

Smart sensors are designed to collect information from one physical quantity to electrical signal. The traditional sensors which were designed consist of three major parts: sensing element which is used to sense the physical quantity, signal conditioning & processing elements is used to for amplification, filtering & to provide the linearization & compensation , sensor interface is used to interface with the external world which has been illustrated in figure 1.

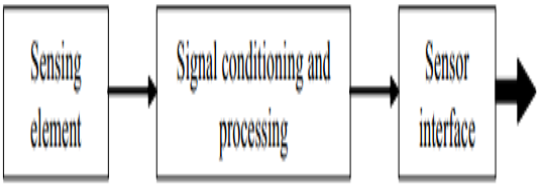

Figure 1: Traditional sensor

The major difference between the traditional sensor & smart sensor is its intelligence, storing data capability, decision making ability which is on board microprocessor. A microprocessor is build with the digital signal processing analog to digital conversion or frequency to code conversion, calculation & interfacing function which provides self diagnostics, identification &self adaption function. The microprocessor base system provides the data storage & controls the power consumption. It is featured with on board CPU small size, wireless capability & low cost which is shown in figure 2. Continuous improvement in upcoming technologies eventually brought other important parameter in picture such as memory & batteries which will allow more capable & reliable devices. Most of the smart sensors are wirelesses that are based on RF communication. These sensors use low radiated power to avoid the heavy costs. The ever growing market of smart sensor is capable of providing services such as configuration, remote diagnosis & real time application. The undesirable characteristics of smart sensors have been reduced due to presence of controllers & processors in building it. Smart sensor improves the cost of by minimizing the set up & by repetitive testing time. Smart sensors are able enhance the self calibration, computation, communication, multisensing. It is able to increase the

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

system reliability as it is capable of finding its flaws & error & produce the consequence. The smart sensors developers are constantly taking efforts to improvise the characteristics of smart sensors such as non linearity, cross sensitivity & offset.

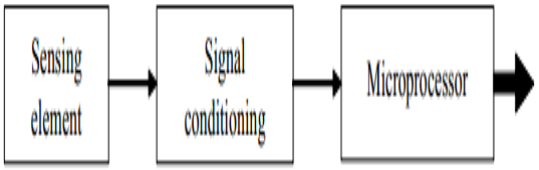

Figure 2: smart sensor using Microprocessor

IEEE 1451 STANDARD

The sensors to the digital world of processors, controllers & networks the IEEE 1451 is approved standard. An effort to overcome the problem that arise while interfacing smart sensor to microprocessor field bus & network has led IEEE 1451 & National Institute Standard Technology to define new set of standards. The aim of this standard is to provide common functionality, network & vendor independent, define transducer electronics data sheet. It does not specify a specific fieldbus protocol but provide specific data sheet of IEEE1451. It supports the introduction of self contained nodes that keep the configuration data physically associated with nodes. The memory requirement is high at IEEE 1451.As it is very difficult to establish communication with digital world hence the major purpose of this standard is to minimize the complexities at designers face. IEEE 1451 enables system design with plug & play modules by stating the bus architecture, addressing protocols, wiring & error correction & calibration. The plug & play concept of IEEE1451 allows liberty to select among sensor, networks & interface modules. These standard is able to produce information related to software model which is object oriented, network independent with standard digital interface & communication protocols for accessing sensor.

3. METHODOLGY

The block diagram of the proposed design is shown in the figure 1.The VHDL model for smart sensor consists of the sensing element, signal conditioning & signal processing blocks. The input to the model is voice signal through the microphone which is interfered with noise signal. This input signal is feed to smart sensor model using VHDL model.

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

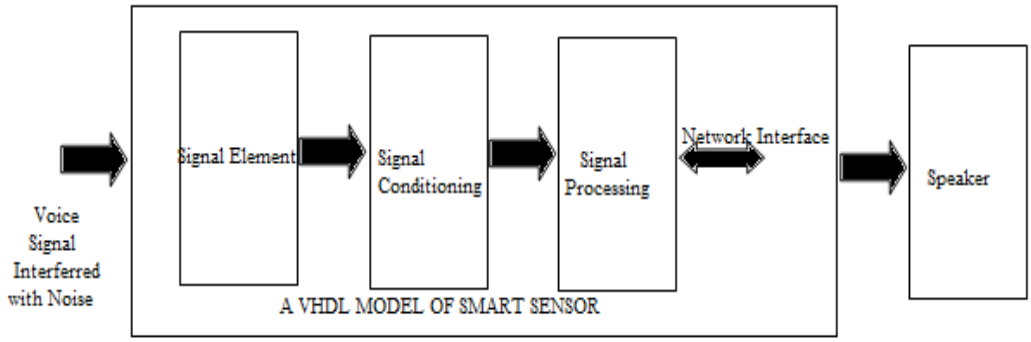

Figure 3: Block Diagram of the smart sensor using VHDL

The sensing element sense the analog signal converts into the digital signal using analog to digital converter. The signal conditioning block consist of amplification, filtering, converting, range matching, isolation and any other processes required making sensor output suitable for processing after conditioning. Signal Processing is usually done to measure, filter and is used to compress continuous real time analog signals. The first step is usually to convert the signal from an analog to a digital form, by sampling and then digitizing it using an analog-to-digital converter (ADC). The required output signal is fed to another analog output signal, which requires a digital-to-analog converter (DAC). A Signal Processing block consist of Program& data memory, compute engine & input & output

4. FILTER STRUCTURE IMPLEMENTATION

In many signal processing application, FIR filters are preferred over the IIR. The main advantages of the FIR filter over their IIE equivalent are the following:

A. Fir filter with exactly liner phase can be easily be deigned.
B. There exists computationally efficient realization for implementing FIR filters. These include both non recursive realizations.
C. FIR filters realizations
D. FIR filters realized non recursively are inherently stable & free of limit cycle oscillations when implemented on finite world length digital system.
E. Excellent design methods are available for various kinds of FIR

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

filters within the arbitrary specifications.

F. The output noise to multiplication round off errors in an FIR filter is usually very low & the sensitivity to variations in the filter coefficients is also low.

REALIZATION OF FIR FILTER

A digital FIR filter can be displayed as shown in Fig.2. This configuration represents convolution invoking N coefficients which are also called as the length of filter. Signal x is the input to the filter & y is the output from the filter as described by Eqn. 1

$$\mathbf{y(n)} = \sum_{k=0}^{N-1} x(n - k)\, ak \qquad (i)$$

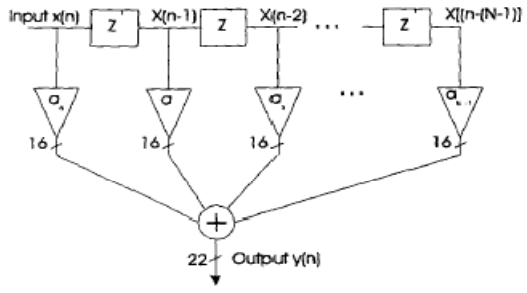

Figure 5: System diagram for general FIR filter implementation

FILTER STRUCTURE

The direct form of an FIRfilter is shown in Fig. 3 which mainly consists of shiftregisters, adders and multipliers. The signal samples aremultiplied by filter coefficients and are gathered togetherin the adder block.

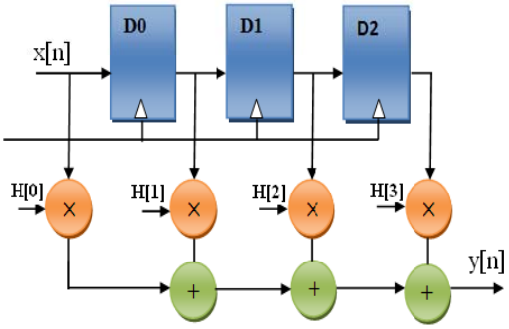

Figure 6: The direct form of FIR filter

CHARACTERISTICS OF LINEAR-PHASE FIR FILTERS

Some properties of linear-phase FIR filters are reviewed in this section, such as the conditions for linear phase and the zero locations of these filters as well as different representation forms for the frequency response.

CONDITIONS FOR LINEAR PHASE

Let {h[n]} be the impulse response of a causal FIR filter of length N+ 1. The transfer function of this filter is

$$H(z) = \sum_{n=0}^{N} h[n] z^{-n} \qquad (ii)$$

The corresponding frequency response is given by

$$H(e^{j\omega}) = \sum_{n=0}^{N} h[n] e^{-j\omega n} \qquad (iii)$$

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VOLUME 02 ISSUE 05 JULY 2014

In the above, N is the order of the filter.

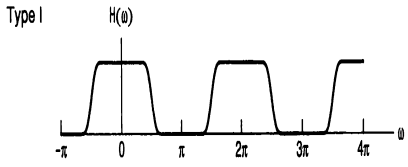

Figure7: Zero Phase frequency response for Type I linear filter

ALGORITHM

a. Analog values for 2^8=256 i.e is ranged -127 to 128 to be defined by constant
b. Absolute values are required for the transducer that's why -127 to 0 values are discarded & only absolute values are kept.
c. Variable defined for 128 bit input.
d. FIR filter of Butterworth type design elements are filter length 129,structure of filter is Direct Form ,Stable, Type -1 linear phase
e. Conversion digital values to analog for further analog display like DSO.

PARALLEL VHDL IMPLEMENTATION

The VLSI chip designs are becoming more complex, it is unrealistic for designers to build and test a prototype of a microelectronic circuit. Therefore, today's chip designers use VHDL. These designers are discovering that sequential execution limits the speed at which a VHDL simulation can be run. By distributing VHDL throughout a parallel processor, designers complete a simulation run more quickly. If each individual simulation is faster, designers are able to perform more tests on different configurations of the circuit. These easily reconfigured C circuits and tests result in a more robust chip design. Iricreasing the reliability of each chip increases the reliability and accuracy of the weapon systems which use these chips. More reliable weapon systems increase the ability to deliver the payload to the intended target and avoid collateral damage.

To develop parallel simulations for VHDL requires familiarity in two distinct areas. The first is simulations in general. One must understand simulation approaches to choose which would be best for modeling the behavior of an electronic circuit. The second area is VHDL itself. One cannot parallelize VHDL without comprehending the interdependencies of sequential VHDL's separate stages.

5. SIMULATION RESULT

The code is written in VHDL & it is stimulated on Xilinx 9.2 version which is depicted in figure.10 which shows the

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

input to smart sensor & figure 11 shows the variation in output. This language is used to describe hardware for the purpose of simulation, modeling, design, testing and documentation. The languages are used to represent the functional and wiring details of digital systems in a compact form. It must uniquely and unambiguously define the hardware at various levels of abstraction. The IEEE standard VHDL is such a language. The figure 8 & 9 below shows the RTL schematic of Smart Senor.

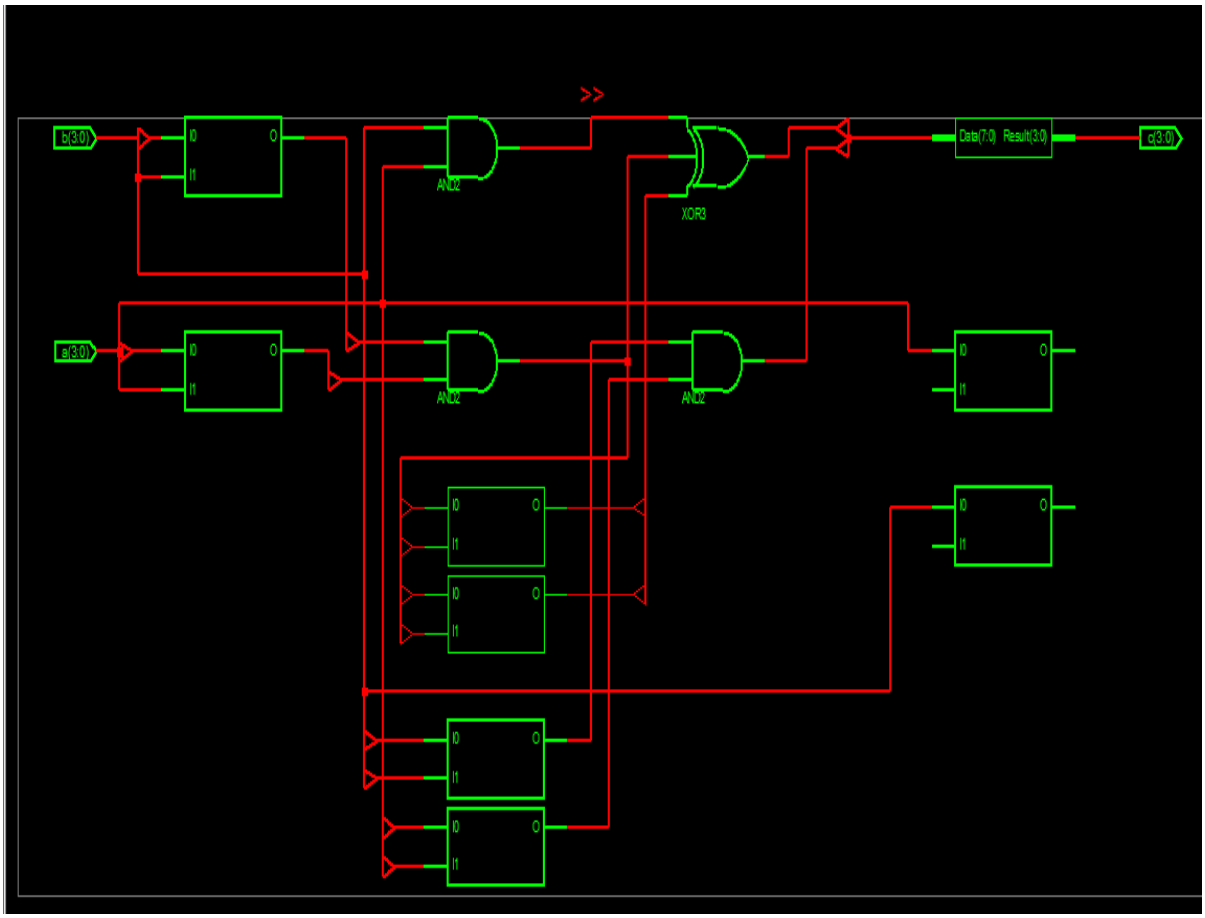

Figure 8: shows the RTL schematic of smart sensor

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

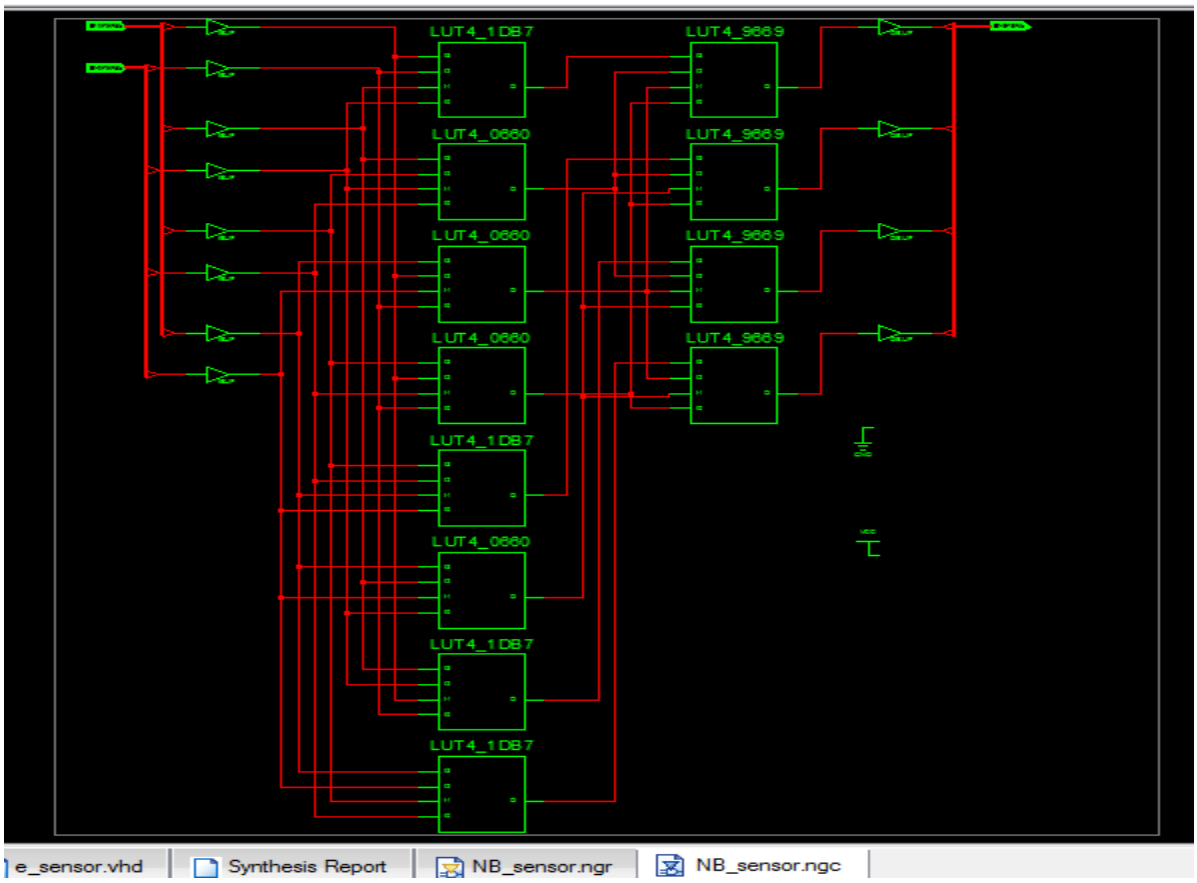

Figure 9: shows the view schematic of smart senor module

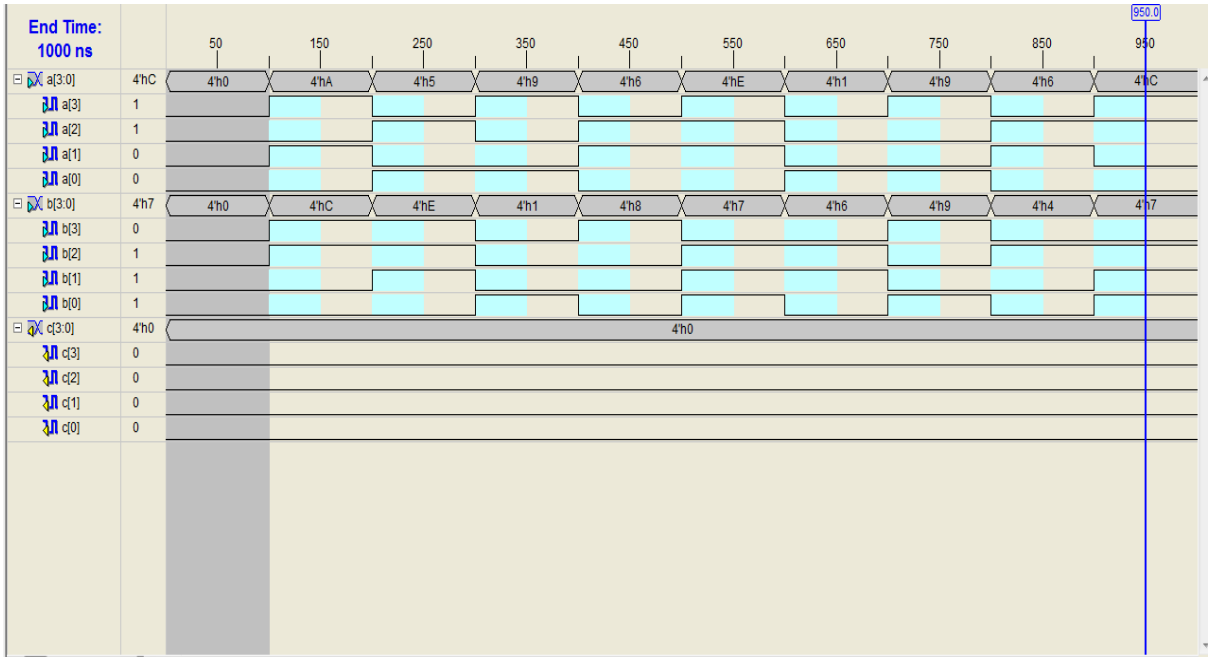

Figure 10: input to smart senor

ISSN: 2348-4098
VOLUME 02 ISSUE 05 JULY 2014

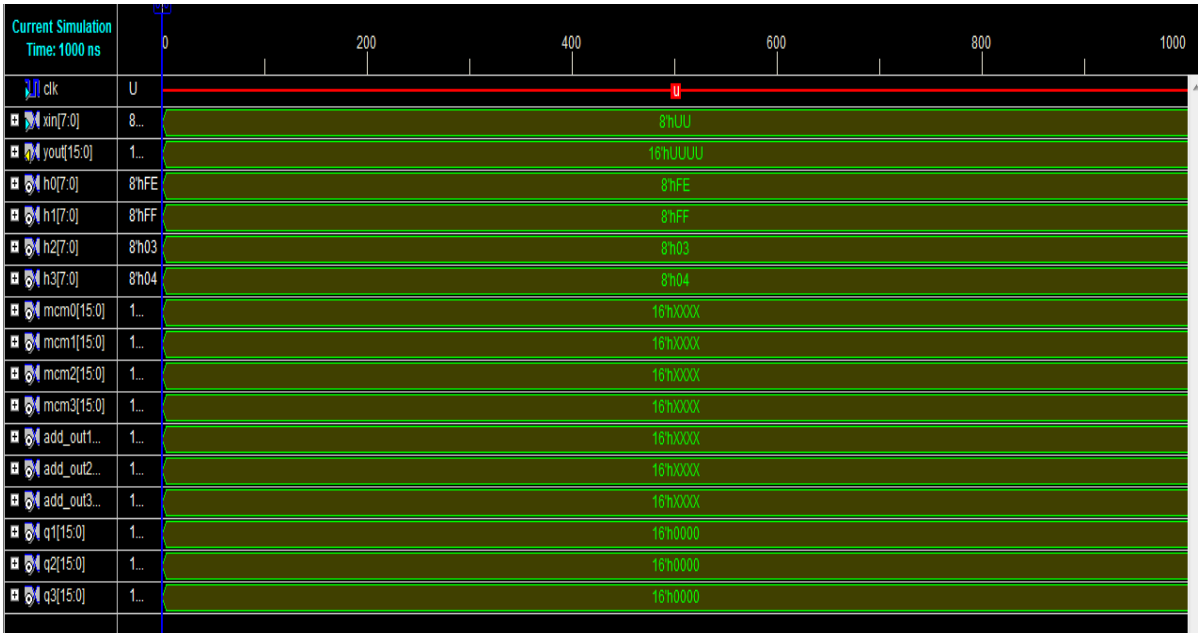

Figure 11: output of smart sensor

6. CONCLUSIONS

The paper focused on the concept of smart sensor, filter implementation, methodology & algorithm to implement the VHDL model of Smart sensor. The standard VHDL is presented which is event driving modeling technique for high simulation for smart sensor implementation, to develop the software model that process the voice signal & reduce the noise signal& thus can be implemented on FPGA kit. This modeling scheme provides fast simulation test and it is useful tool for generating an integrated smart sensor.

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