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Review of Reversible Realization of Adder Subtractor Circuit

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Abstract- Reversible logic computation is one of the most essential promising technologies in designing low-power digital circuits, optical information processing, quantum dot cellular automata, fault tolerant system and nanotechnology. In fact, the conventional digital circuits dissipate a significant amount of energy because several bits of information are deleted during the treatments. In reversible computation, the information bits are not lost. This paper presents the study of reversible realization of adder-subtractor circuit.

Keywords- Digital, Reversible, Realization, Adder, Subtractor.

I. INTRODUCTION

Reversible computation is a heavily investigated emerging technology due to its promising characteristics in low power design, its application in quantum computations, and several further application areas. The currently established functional synthesis flow for reversible circuits is composed of two distinct steps. First, an embedding process is conducted which makes no unique output patterns distinguishable by adding further variables.

Then, this function is passed to a synthesis method which eventually yields a reversible circuit. However, the separate consideration of the embedding and synthesis tasks leads to significant drawbacks. In fact, embedding is not necessarily conducted in a fashion which is suited for the following synthesis process. In addition, embedding adds further variables to the function to be synthesized which exponentially increases its corresponding representation in the worst case.

An important component of quantum processing is reversibility, since advancement of a quantum framework is portrayed by a unitary operator and thus it is reversible. Quantum cost is another important factor of any reversible circuit.

The most minimal quantum cost demonstrates the least cost of reversible circuit. By most reduced quantum cost can make a quantum PC.

In this paper we tell the best way to locate the most minimal quantum cost and demonstrate a progressed Toffoli Gate that contains least quantum cost Quantum cost, the cost of a circuit, alludes to the general costs, relating to the utilization of Reversible Logic Gates for incorporating a given logical capacity, brought about in structuring of the circuit regarding the cost of the crude Reversible Logic Gates utilized.

The quantum cost of the circuit is controlled by computing the definitely realized cost of the crude gates required for understanding the Number juggling and Logic circuit units. Some work presents 3*3 reversible gate to be specific Progressed Toffoli gate, that is, it has 3-input lines and 3-output lines. The fundamental alluring component of this gate is quantum cost.

It has a 3 quantum cost which is less than 5 quantum cost. It works under certain conditions and application might be same as customary traditional Toffoli gate.

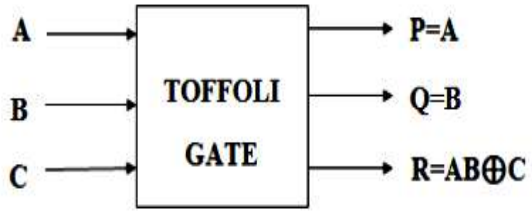

Fig 1. Toffoli Gate.

II. LITERATURE SURVEY

V. Shukla et. al., [1] propose an efficient approach to design N-bit Adder/subtractor using reversible approach. Based on proposed N-bit Adder/ Subtractor design it have also compared 4-bit, 8-bit and 16-bit circuits with the existing designs. Proposed designs are simulated and synthesized with Xilinx Spartan 3E for Device XC3S500E at 200 MHz frequency.

V. P. Singh et. al., [2] presents two designs of reversible circuit are proposed. These circuits can be used as an Adder as well as a Subtractor. These circuit also generate carry and borrow propagate signal to predict carry and borrow for faster add and subtract operations. At input these circuits contains one control signal and three input bit signals.

There are three output signals namely sum or difference signal, carry or borrow signal and carry propagate or borrow propagate signal. Constant inputs and Garbage outputs are also present to maintain reversibility but they are minimized up to possible extent. However proposed designs can be implemented in carry skip Adders and borrow skip subtractor. As a result proposed designs are faster than some existing designs.

S. S. Kumar et. al., [3] Residue Number System (RNS) supports carry-free computations and improves the speed of arithmetic circuits. Modulo is an RNS operation. Conventional modulo 2 n +1 subtractor and adder/subtractor architectures employing different adder structures are presented in this work. Modulo arithmetic circuits operate on operands in normal and diminished-one representations. Operands of length 4-bits and 8-bits were considered. Subtractor and combined adder/subtractor architectures were analyzed and compared for area and delay parameters.

S. S. Ramachandran et. al., [4] presents design of the QCA-based half and full subtractor has an area of 0.06 µm 2 and 0.10 µm 2 respectively which is better to those conventional subtractors occupying an area of 0.13 µm 2 and 0.17 µm 2 respectively. Also this modified half and full subtractor has 38 and 83 cells respectively while the conventional half and full subtractor has 93 and 122 cells respectively. The half and full subtractor are made using 5 input majority gate along with the combination of basic gates.

V. Shukla et. al., [5] presents two design approaches for reversible realization of 8-bit adder-subtractor circuit with optimized quantum cost. These designs are compared with existing designs on some selected performance parameters such as total number of reversible gates, garbage outputs and quantum cost. The proposed design for 8-bit adder-subtractor circuit using reversible approach simulated using Modelsim tool and synthesised for Xilinx Spartan 3E with Device XC3S500E with 200 MHz frequency. This optimized circuit may be utilized further for the designing of low power computing devices.

V. Shukla O. P. Singh et. al., [6] presents an approach to design n-bit adder/subtractor circuits with available reversible logic gates only. The proposed design is compared with existing designs based on some selected factors such as total number of reversible gates used in the design, garbage outputs generated and quantum cost of the design. Based on the proposed design approach, 8-bit adder-subtractor circuit using reversible approach is simulated and synthesised for Xilinx Spartan 3E with Device XC3S500E with 200 MHz frequency. Application of this optimized circuit may be visualized for the designing of low power processing devices.

K. Ghosh et. al., [7] These circuits are very essential for the construction of various computational units of quantum computers and other complex computational systems. Design of reversible circuits can be improved by reducing the quantum circuit cost. This work uses some elementary components and typical ternary gates (generalized ternary gate, M-S gate etc.) to perform arithmetic addition, subtraction and encoding operations. Finally, it evaluates the optimum cost for each circuit.

M. Sangsefidi et. al., [8] In this work, a new layout of XOR gate is presented in QCA technology, then, it is exploited to design an 8-bit controllable inverter. Finally, using the proposed design and last adder circuit provided by ourselves in our previous work, an 8-bit adder/subtract or is designed. It is the most important component of an ALU. All the designed circuits have used coplanar clock-zone based crossover. The most prominent characteristics of designed circuits include very high operation speed, very low complexity, small area, completely coplanar design, and also avoiding rotated cells in us designs

for Avoidance of Construction Challenges QCA Circuits. The mentioned characteristics are considerably improved in our proposed structure comparing to its counterparts. The proposed structure is verified and evaluated in QCA framework using QCA Designer Ver.2.0.3 software.

R. Bardhan et. al., [9] presents an efficient adder/subtractor circuit using QCA 3-dot cell. This model is highly proficient to compute both addition and subtraction operations. it is also showed here a strong subtractor circuit. Moreover, our new and novel schemes have least number of QCA cells till now.

The proposed designs carry out more beneficiary than the present ones, e.g., the proposed 32-bit subtractor circuit improves 73% on QCA cell, 99% on area and the proposed 32-bit adder/subtractor circuit improves 90% on QCA cell, 99% on area than the existing best known one.

N. J. Lisa et. al., [10] present an optimized design for the quantum ternary adder/subtract or circuit. it is propose the design of quantum Ternary Peres Gate (TPG). The design of our proposed quantum ternary adder/subtract or circuit consists of two parts: a) Firstly, it has the design of a quantum ternary full-adder circuit using the proposed TPG gates, and b) Secondly, it designs the proposed adder/subtract or circuit by using the constructed full-adder in a) and M-S gates. it is also propose a heuristic to design a compact ternary adder/subtract or circuit. Our circuits perform much better than the existing ones.

A. K. Chowdhury et. al., [11] reversible computation has received much attention in the field of low power circuit design. In this work, an irreversible IG-A gate is presented. The gate is further used to design irreversible full adder/subtractor (IAS). Furthermore, IAS block is utilized to construct n-bit adder and subtractor. Proposed IAS design is analyzed and compared against the existing reversible methods. Features such as, hardware cost, logic calculation and gate count are investigated to show the efficiency of the design.

Transistor level design and simulation of IG-A circuit are shown using Cadence Or CAD Lite. The one-bit IAS simulation results are verified using Altera Quartus II and ModelSim software. Simulation results show that the circuit offers reduced hardware complexity as compared to the existing reversible full adder design.

A. Rahman et. al., [12] presents a new, efficient hardware design methodology for implementing double precision floating point addition and subtraction. The pipeline hardware design is implemented on Virtex-6 and Virtex-5 Xilinx FPGA. As per the synthesis result, the maximum operating frequency achieved for the proposed hardware design for clock latency of 8 cycles is significantly higher than the previous hardware designs. Furthermore, area overhead is 50 percent fewer than that of the earlier proposed hardware designs for computing IEEE 754 compliant double precision floating point addition and subtraction.

III. CONVENTIONAL FULL ADDER CIRCUIT

The fundamental entity that needs to be created is the Full Adder. The purpose of this entity is to find the sum and carry when two 1-bit numbers are added. Though a full adder can be constructed in more than one way, the AND-OR-Invert (AOI) studied.

This entity has three 1-bit inputs and two 1-bit outputs: a and b (the numbers to be added), c_in (the carry in, also added), c_out (the carry out), and s (the sum of a+b+c_in).

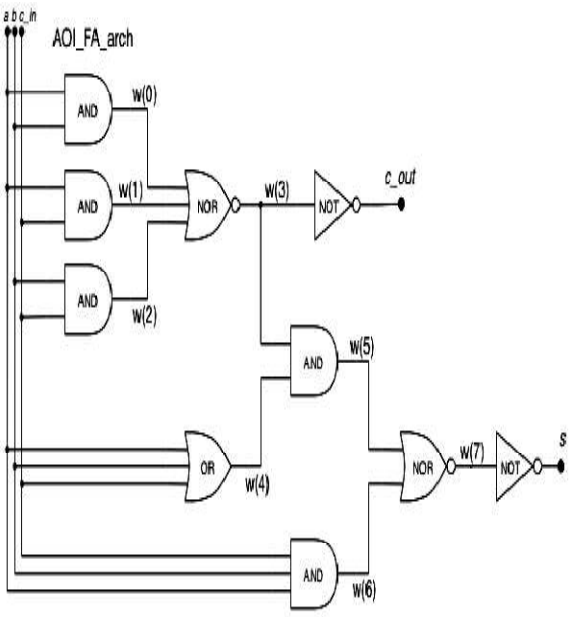

Fig 2. Full adder.

Before proceeding further the terms carry and sum should be clearly defined, which can be best done through an example. Consider the addition of the following decimal numbers: 5+6. When adding this decimal number, we cannot correctly represent the number "11" in the 1s place, so we carry a 1 to the 10s place, leaving a sum of 1 in the ones place.

An equivalent process occurs for binary. When adding 1+1 in binary, you cannot represent "2" in the 1s place, so you carry a 1 to the 2s place, leaving a sum of 0. This is the case with the full adder. The sum (*s*) represents the remainder of the total sum *a+b+c_in*, after a carry (*c_out*) has been made, if necessary. The purpose of the full adder then is to find the sum of two 1-bit numbers and a 1-bit carry in.

The AOI_FA entity was written using dataflow, joining inputs with Boolean operators such as "and", "or" and "not." There is more than one way to construct the AOI_FA using VHDL dataflow descriptions. This project described each gate individually, connecting the output of one gate to the input of another using a wire. Alternately the outputs *c_out* and *s* could have been described as a combination of operators in a longer concurrent statement, reducing the number of internal wires needed. This project chose to represent each gate individually to reduce possibility for error when writing a single long concurrent statement. The entity AOI_FA is shown in Figure 3.

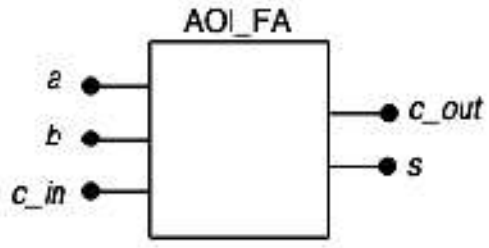

Fig 3. AOI_FA

After constructing the AOI_FA shown in Figure 4 using VHDL, we must test its function. Since there are three inputs to the entity, there are 23 unique combinations of inputs to test.

IV. CONCLUSION

Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat.

This paper reviews of the reversible realization of adder-subtractor circuits. The lowest level entities, XOR_GATE and AOI_FA, were described using the dataflow method. These entities were combined together using the structural description method to make a 1-bit adder/subtractor, which was repeated and ultimately created the 8-bit adder/subtractor.

REFERENCES

[1] V. Shukla, O. P. Singh, G. R. Mishra and R. K. Tiwari, "Design and performance analysis for the reversible realization of adder/subtractor circuit," 2017 International Conference on Emerging Trends in Computing and Communication Technologies (ICETCCT), Dehradun, 2017, pp. 1-6.

[2] V. P. Singh and M. Rai, "Reversible adder-subtractor circuit with carry and borrow propagate facility," 2017 3rd International Conference on Advances in Computing, Communication & Automation (ICACCA) (Fall), Dehradun, 2017, pp. 1-6.

[3] S. S. Kumar and B. Kala, "Performance analysis of modulo 2n+1 subtractor and combined adder/subtractor architectures," 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), Chennai, 2017, pp. 736-741.

[4] S. S. Ramachandran and K. J. J. Kumar, "Design of a 1-bit half and full subtractor using a quantum-dot cellular automata (QCA)," 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), Chennai, 2017, pp. 2324-2327.

[5] V. Shukla, O. P. Singh, G. R. Mishra and R. K. Tiwari, "A novel approach for reversible realization of 8-bit adder-subtractor circuit with optimized quantum cost," 2016 International Conference on Emerging Trends in Engineering, Technology and Science (ICETETS), Pudukkottai, 2016, pp. 1-6.

[6] V. Shukla, O. P. Singh, G. R. Mishra and R. K. Tiwari, "Performance parameters optimization

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and implementation of adder/subtractor circuit using reversible logic approach," 2016 11th International Conference on Industrial and Information Systems (ICIIS), Roorkee, 2016, pp. 323-328.

[7] K. Ghosh, M. M. Haque and S. Chakraborty, "Design of reversible ternary adder/subtractor and encoder/priority encoder circuits," 2016 International Conference on Communication and Signal Processing (ICCSP), Melmaruvathur, 2016, pp. 1290-1295.

[8] M. Sangsefidi, M. Karimpour and M. Sarayloo, "Efficient Design of a Coplanar Adder/Subtractor in Quantum-Dot Cellular Automata," 2015 IEEE European Modelling Symposium (EMS), Madrid, 2015, pp. 456-461.

[9] R. Bardhan, T. Sultana and N. J. Lisa, "An efficient design of adder/subtractor circuit using quantum dot cellular automata," 2015 18th International Conference on Computer and Information Technology (ICCIT), Dhaka, 2015, pp. 495-500.

[10] N. J. Lisa and H. M. H. Babu, "Design of a Compact Ternary Parallel Adder/Subtractor Circuit in Quantum Computing," 2015 IEEE International Symposium on Multiple-Valued Logic, Waterloo, ON, 2015, pp. 36-41.

[11] A. K. Chowdhury, D. Y. W. Tan, S. L. B. Yew, G. L. C. Wyai, B. Madon and A. Thangarajah, "Design of full adder/subtractor using irreversible IG-A gate," 2015 International Conference on Computer, Communications, and Control Technology (I4CT), Kuching, 2015, pp. 103-107.

[12] Rahman, Abdullah-Al-Kafi, M. Khalid, A. T. M. S. Islam and M. Rahman, "Optimized hardware architecture for implementing IEEE 754 standard double precision floating point adder/subtractor," 2014 17th International Conference on Computer and Information Technology (ICCIT), Dhaka, 2014, pp. 147-152.