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VHDL Based Design of Convolutional Encoder Using Vedic Mathematics and Viterbi Decoder

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Abstract- As in mathematics, multiplication is the most used operation. An ancient Vedic sutra named 'urdhavtriyagbhyam' is used for multiplication which gives a difference in actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. This paper presents the design of convolution encoder using vedic mathematics and Viterbi decoder using parallel processing. The coding follows a fast multiplication process and achieves a less computational complexity over its conventional multiplier resulting in a smaller number of devices utilization. Convolution encoding with Viterbi decoding is a good forward error correction technique suitable for channels affected by noise degradation. The simulation and synthesis of proposed design are done through XILINX 14.2i ISE simulator tool and coding is in Verilog with Spartan 3A as the target FPGA.

Keywords- Convolution encoder, Vedic mathematics, Urdhav triyagbhyam, Viterbi decoder.

I. INTRODUCTION

Noise in a communications channel can cause errors in the transmission of binary digits.

For some types of information, errors can be detected and corrected but not in others.

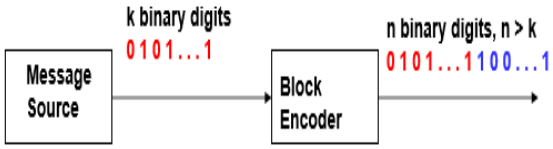
In binary error correcting codes, only certain binary sequences (called code words) are transmitted.

Binary Error Correcting Codes (ECC):

- 2k equally likely messages can be represented by k binary digits.
- If these k digits are not coded, an error in one or more of the k binary digits will result in the wrong message being received.
- Error correcting codes is a technique whereby more than the minimum number of binary digits is used to represent the messages.
- The aim of the extra digits, called redundant or parity digits is to detect and hopefully correct any errors that occurred in transmission.

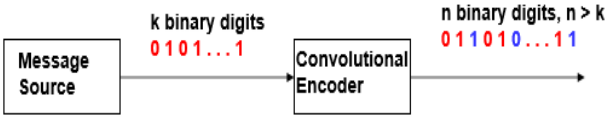
2. Types of Binary Codes:

2.1 Block Codes:



Rate = k / n

2.2 Convolution Codes:



Rate = k / n

Convolution codes offer an alternative to block codes for transmission over a noise channel. In block codes, (k) information symbols are encoded into block of (n) coded symbols.

Drawback of having very large block length is that, until the entire block of encoded data is received at the receiver, the decoding procedure cannot start, which results in delays. In convolution code decisions are made based on past information hence memory is required.

II. CONVOLUTION ENCODER

The encoder is a device that converts information from one format or code to another for the purpose of speed. Convolution encoding is one of the forward error correction schemes. Error correction technique improves the capacity by adding redundant information for the source data transmission.

It provides an alternative approach to block codes for transmission over a noisy channel. Convolution code is defined by three parameters, (n.k,K) where 'n' is the number of output bits, 'k' is number of input bits and 'K' is constraint length. In convolution encoder technique, condition is that number of input bits 'k'must be less than output 'n' of convolution encoder.

III. VEDIC MULTIPLICATION

Multiplication is most important function in arithmetic operations. Since multiplication decreases the execution time of most algorithms, hence there is a need of high speed multiplier.

The Vedic mathematics is very different method which reduces human mind work. Vedic mathematics is a name given to ancient system of mathematics, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved like arithmetic, algebra, geometry or trigonometry. Performing arithmetic calculations especially multiplication, a computer spends a considerable amount of its processing time, an improvement in the speed for performing multiplication will increase overall speed of the computer.The multipliers used in convolution encoder are based on Vedic mathematics. The word Vedic is derived from the word Veda which means the store house of all knowledge.

There are! 6 sutras in Vedic multiplication in which "urdhavtiryakbhyam" has been noticed to be the most efficient one in terms of speed. A large number of high speed vedic multipliers have been proposed with urdhavtriyakbhyam sutra. Vedic multiplier is one of the fastest and low power multiplier.

The sutra is based on "vertically and crosswise" technique. The advantage of multiplier based on this sutra over other is that with the increase in number of bits area and delay increases at smaller rate in comparison to others.

IV. EXPERIMENTAL RESULTS

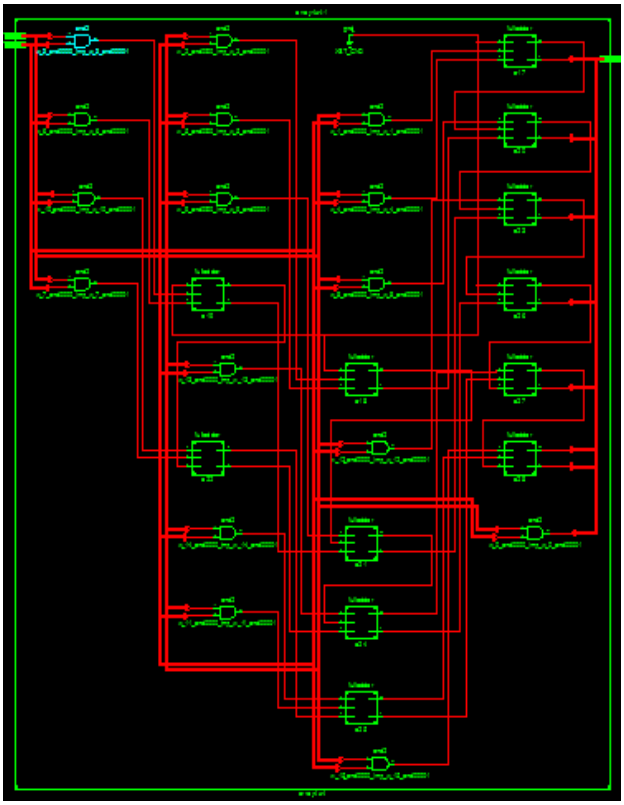


Fig 1. Technology Schematic of Convolution Encoder.

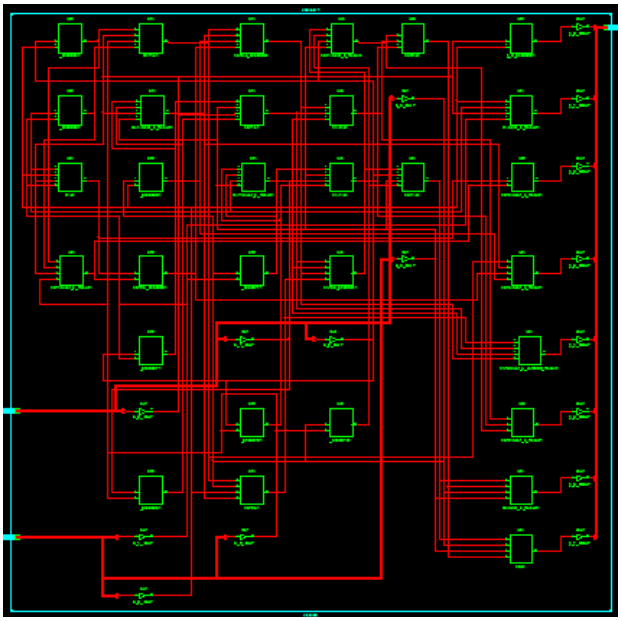


Fig 2. Technology Schematic of Vedic Encoder.

V. SIMULATION RESULT

Fig 31 TBW of Vedic Encoder.

Fig 4. TBW of Viterbi Decoder

VI. CONCLUSION

In this paper, the design and simulation of the convolution encoding using Vedic mathematics is done. This design has been synthesized and simulated on SPARTAN 3A using XILINX 14.2i IES simulator. The architecture is efficient in speed and area and is flexible in design. The same architecture can be extended for more no. of bits.

Convolution encoder using Vedic multiplier improves delay and provides faster speed than the normal convolution encoder. It enables parallel generation of partial products and eliminates unwanted multiplications steps. The algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its counterpart. For the basic design of the codes can be developed based on code rate and constraint length.

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