Jayanti lodhi, 2023, 11:4
ISSN (Online): 2348-4098
ISSN (Print): 2395-4752

Design And Performance Evaluation Of A Low-Power CMOS LC VCO For High-Frequency Applications

M.Tech. Scholar Jyanti lodhi
Dept of Electronics and Communication Engineering
Eklavya university,Damoh,mp,India

Abstract- This paper presents the design of a Low Power CMOS LC Voltage Controlled Oscillator (VCO) specifically optimized for C-band applications. The design incorporates a cross-coupled differential LC VCO topology, carefully balancing the trade-off between phase noise and power consumption. The circuit is implemented using a 70nm CMOS technology, making it suitable for wireless applications. To achieve a wide frequency tuning range, a variable MOS capacitance is employed by modulating the gate voltage of the MOS transistor, which aligns with the requirements of the C-band applications. The simulation is carried out using Tanner EDA 14.0 on the 70nm CMOS technology. The tuning frequency of the LC VCO circuit spans from 4.99 to 5.38 GHz, achieved by applying a tuning voltage ranging from 1.5 to 2.7 V. Remarkably, this VCO topology exhibits a significantly low power dissipation of 1.40mW at its maximum oscillation frequency, surpassing conventional VCO designs in terms of power efficiency.

Keywords- Voltage Controlled oscillator (VCO), tuning frequency, tuning range, power consumption, CMOS

I. INTRODUCTION

Oscillators are essential components in various electronic systems and have diverse applications, ranging from generating clock signals in microprocessors to synthesizing carriers in cellular mobile communication. The continuous advancements in complementary metal oxide semiconductor (CMOS) technology, coupled with the rapid growth of wireless communication, have made it possible to implement high-frequency oscillators using CMOS technology. In wireless communication

systems, oscillators need to be tunable over a wide frequency range to accommodate different frequency requirements. This tunability is achieved through Voltage Controlled Oscillators (VCOs), which allow for frequency variation by adjusting the voltage applied to them. VCOs are particularly crucial in frequency synthesizers used in wireless communication applications, where they are responsible for tasks such as frequency selection and carrier generation. One common approach for achieving programmable carrier frequencies in RF transceivers is through the use of phase-locked loops (PLLs), which incorporate an RF oscillator with controllable frequency. These PLLs rely on the precise control of the VCO's frequency to achieve accurate frequency synthesis and modulation in wireless communication systems. [1-2] The performance of a VCO is characterized by its phase noise, tuning range, and power consumption, which are critical factors in VCO selection. Both ring VCO and LC VCO topologies exhibit desirable performance characteristics. However, for wireless applications, where low phase noise and power consumption are crucial, LC VCOs are preferred due to their inherent filtering capabilities, ensuring significantly reduced phase noise. [3]

Numerous topologies for designing LC VCOs have been documented [4-6], including single-transistor oscillator topology, cross-coupled differential topology, CMOS core cross-coupled differential

International Journal of Science, Engineering and Technology

An Open Access Journal

topology, and quadrature VCO with reconfigurable LC VCO. While the single-transistor topology has a larger transistor area compared to the cross-coupled differential topology, the latter is considered more accurate for fully integrated CMOS VCOs. CMOS core cross-coupled topology exhibits higher parasitic capacitance, leading to reduced tuning range, making it less suitable for high-frequency wireless applications. [7-13] In [14], a proposed wideband LC VCO employs a switched capacitor array, substrate noise filter, and two power supplies within the CMOS differential cross-coupled topology, aiming for low phase noise and power consumption in wireless applications.

This paper introduces a cross-coupled differential topology for high-frequency applications with low power consumption. The objective of this design is to achieve high-frequency operation and low power consumption using 70nm CMOS technology without the need for a switched capacitor array or two power supplies.

The remaining sections of the paper are organized as follows: Section II discusses the basic feedback amplifier model for oscillators and Barkhausen criteria for oscillation. Section III presents the proposed cross-coupled differential topology and simulation results. A comparison of simulation results is provided in Section IV, followed by the conclusion in Section V.

II. FEEDBACK MODEL OF OSCILLATOR

An oscillator is a device that generates a periodic voltage output. Although oscillators exhibit nonlinearity, they are commonly represented as linear time-invariant feedback systems, as depicted in Figure 1. In the s-domain, the transfer function of this negative feedback amplifier system can be expressed as:

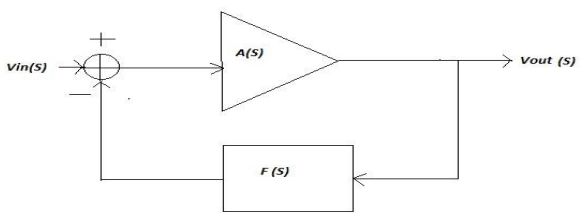

Fig.1. Negative feedback system with frequency-selective network.

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)F(s)}$$

This system produces a periodic output at a frequency S = jω0. If the loop gain A(s)F(s) is equal to -1 at a specific frequency ω0, the closed-loop gain approaches infinity. In this scenario, the circuit amplifies its own noise component indefinitely, leading to system instability. In summary, a negative feedback circuit becomes an oscillator if it meets two conditions:

$$|A(j\omega_0)F(j\omega_0)| \geq 1$$
$$\angle |A(j\omega_0)F(j\omega_0)| = 180$$

According to [1], the Barkhausen Criteria for oscillation is necessary but not alone sufficient.

3. Cross Coupled Transistor Topology

The circuit design we are discussing incorporates several key components arranged in a parallel combination. These components include an LC tank lossy section, a cross-coupled NMOS transistor pair, a current mirror, and a variable capacitor. The LC tank section comprises a capacitor (C), an inductor (L), and a parallel resistance (Rp). The purpose of the cross-coupled MOS transistor pair is to introduce an equivalent negative resistance that compensates for the LC tank's parallel resistance. This compensation is essential for achieving optimal performance.

To ensure low noise characteristics, a PMOS cross-coupled transistor pair is chosen for the VCO design. PMOS devices are preferred in this case due to their minimal hot carrier effects, which is of utmost importance in CMOS processes where hot electron noise can have a significant impact. Additionally, PMOS devices exhibit approximately 10 times lower flicker noise compared to NMOS devices with equal transistor dimensions. The lower flicker noise can be attributed to the PMOS transistor's lower mobility, resulting in reduced noise levels for a given current and gm (transconductance), particularly when a larger gate area is utilized. These advantages make the cross-coupled PMOS pair an excellent choice for achieving low phase noise characteristics. However, it should be noted that PMOS devices need to be twice the size of NMOS devices to achieve comparable transconductance parameters. As a result, in this particular topology, the NMOS cross-coupled pair

International Journal of Science, Engineering and Technology

An Open Access Journal

transistor device is preferred over the PMOS cross-coupled pair transistor device [16-18].

In order to control the negative resistance and oscillation amplitude effectively, a current mirror is commonly employed in the circuit. The primary function of the current mirror is to limit the supply current, providing control and stability to the oscillator. The bias current flowing through the current mirror, often referred to as the tail current, plays a crucial role in determining the overall power dissipation of the circuit. However, it is worth mentioning that in some cases, it has been observed that eliminating the tail current source can lead to improved phase noise characteristics. This suggests that tail current removal may be advantageous in certain scenarios, allowing for further optimization of the VCO's performance [6].

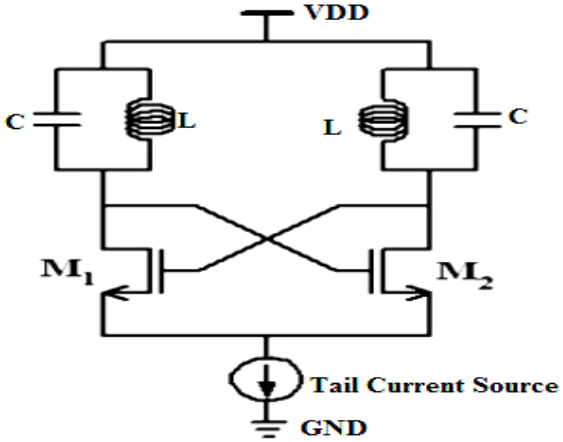

Fig.2. Cross coupled differential topology

4. VCO DESIGN

1. MOS Varactor

In the proposed topology, the MOS capacitor exhibits a structure similar to that of a parallel plate capacitor, with the source, drain, and bulk regions (referred to as D, S, and B) playing significant roles. In this configuration, a PMOS transistor is interconnected to form one of the capacitor plates, while the polysilicon gate serves as the other plate. This arrangement results in the formation of a MOS capacitor, as depicted in Figure 3.

The MOS capacitor is an essential component in MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) devices, and its structure plays a crucial role in the overall functionality and performance of the transistor. By modulating the voltage applied to the gate terminal, the capacitance of the MOS capacitor can be effectively controlled, influencing the transistor's behavior and characteristics. The MOS capacitor's ability to store and release electrical charge is fundamental to the operation of MOSFETs and contributes to their numerous applications in integrated circuits and electronic systems. Figure 3 provides a visual representation of the resulting MOS capacitor in this proposed topology, showcasing its distinctive structure and its importance in the overall circuit design.

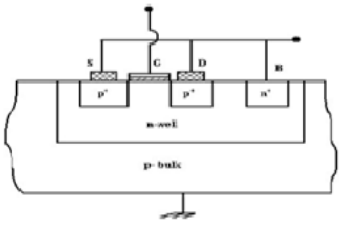

Fig.3. MOS Capacitor.

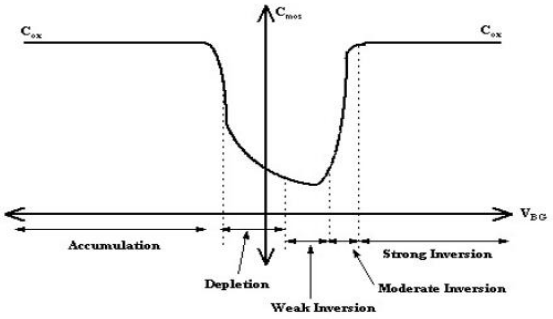

Fig.4. Capacitance versus voltage characteristics

2. Final Proposed VCO Design

The schematic circuit diagram of the proposed LC VCO is visually presented in Figure 5. This circuit design adopts an NMOS cross-coupled differential LC structure (N-pair) with an NMOS transistor serving as the tail current source. The chosen topology has undergone optimization to ensure superior performance compared to other commonly used VCO topologies, particularly in terms of power consumption and high-frequency operation for RF applications.

The optimization process aims to maximize the efficiency and effectiveness of the circuit, enabling it to meet the demanding requirements of RF applications. The proposed circuit design exhibits enhanced power efficiency and frequency capabilities, positioning it as a favorable choice for implementing VCOs in RF systems. By utilizing this optimized circuit topology, the overall performance

International Journal of Science, Engineering and Technology

An Open Access Journal

and functionality of the VCO can be significantly improved. It is important to note that the quality and impact of your research publication can be enhanced by presenting a well-structured and optimized circuit design, providing valuable insights to the scientific community and furthering the advancement of the field. Thank you for your cooperation and valuable contribution to the journal.

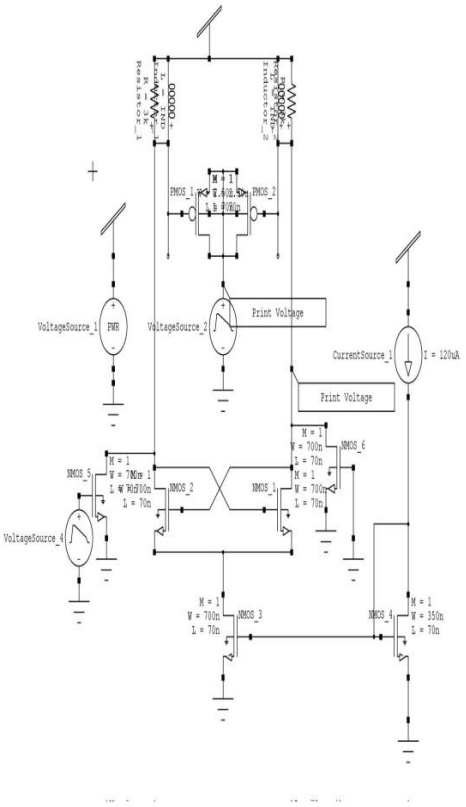

Fig.5. Proposed crossed coupled differential LC VCO topology.

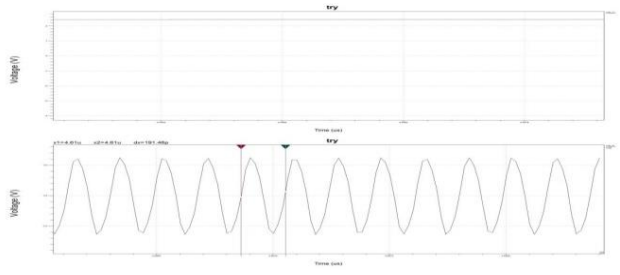

Fig.6. Simulation result of Proposed crossed coupled differential LC VCO topology

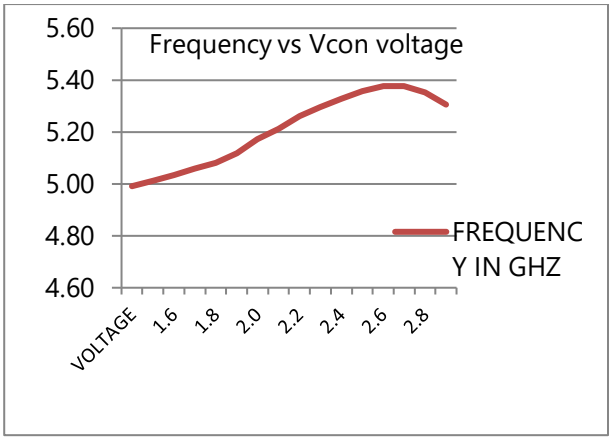

Fig.7. Frequency vs. v_{con} voltage plot.

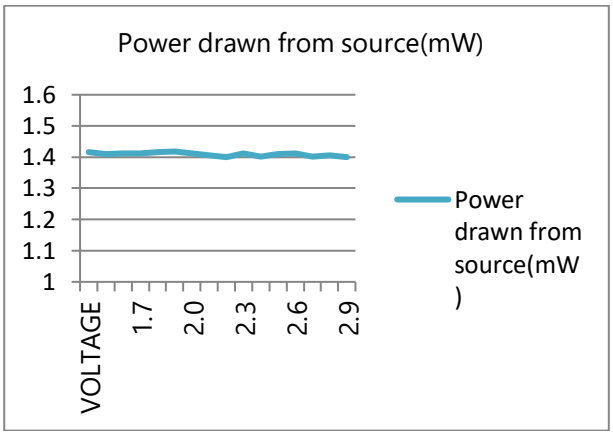

Fig.8. Power drawn from the Source

V. COMPARISON AND DISCUSSION

The accompanying table presents a comprehensive comparison between the current work and previous designs that aimed to achieve a wide tuning range. Upon analyzing the table, it becomes evident that the cross-coupled differential LC VCO topology employed in this study exhibits distinct advantages, particularly in terms of low power consumption and high frequency performance, specifically tailored for C band applications.

The comparison table serves as a valuable tool for evaluating and contrasting the performance of various VCO designs, thereby highlighting the strengths of the proposed cross-coupled differential LC VCO topology. Notably, this topology stands out due to its remarkable power efficiency, consuming minimal power resources during operation. Such low power consumption is of great significance as it contributes to energy conservation, prolongs battery life in portable devices, and promotes sustainable

operation in power-constrained scenarios. Furthermore, the high-frequency capability of the cross-coupled differential LC VCO topology enables reliable operation within the C band frequency range. The C band, being widely used in various wireless communication applications, demands VCOs that can operate at high frequencies while maintaining signal integrity and stability. The ability of the proposed topology to deliver such high-frequency performance positions it as an ideal choice for C band applications.

The inclusion of this comparison table in the research paper provides readers with a clear visualization of the distinct advantages offered by the cross-coupled differential LC VCO topology. By highlighting its low power consumption and high-frequency performance in a concise manner, the table reinforces the significance of the current work and underscores its superiority over previous designs in achieving wide tuning ranges for C band applications.

TABLE 1 .COMPARISON OF PARAMETER

Mode	This Work	Ref.14
Technology	70nm	65nm
Frequency(in GHz)	4.99-5.38	0.75-1.5
Power Consume	1.4 mW	3.4mW
Tuning Range	1.5-2.7	83%
TuningVoltage	7.18	--

VI. CONCLUSIONS

In this study, a low power high frequency cross-coupled differential LC VCO topology is implemented using Tanner 14.0 software on a 70nm CMOS technology platform, specifically designed for C band applications. The VCO demonstrates an impressive tuning frequency range, spanning from 4.99 to 5.38 GHz, achieved by applying a tuning voltage within the range of 1.5 to 2.7 V. Notably, this topology operates with a power consumption of only 1.4mW. The key advantage of this proposed cross-coupled differential LC VCO topology lies in its ability to provide low-power operation while maintaining high-frequency performance suitable for wireless applications. Low power consumption is a crucial requirement in modern electronic systems, as it enhances energy efficiency and contributes to extended battery life, reducing the overall power demands of wireless devices. By minimizing power consumption, the VCO becomes more sustainable and cost-effective in wireless communication applications. Additionally, the high-frequency operation of the cross-coupled differential LC VCO topology makes it well-suited for wireless applications within the C band frequency range. The C band is widely utilized in various wireless communication systems, including satellite communication, radar systems, and wireless local area networks.

By offering high-frequency capability, the VCO ensures reliable and efficient signal generation within this frequency range, enabling seamless communication in C band applications. By implementing this low power high frequency cross-coupled differential LC VCO topology, the study provides a valuable solution for wireless applications that demand both low-power operation and high-frequency performance. The achieved tuning frequency range, tuning voltage range, and power consumption highlight the effectiveness and practicality of the proposed topology, solidifying its potential as a suitable choice for C band applications in the wireless communication domain.

REFERENCES

[1] J. Lannacci, "Internet of things (IoT); internet of everything (IoE); tactile internet; 5G – A (not so evanescent) unifying vision empowered by EHMEMS (energy harvesting MEMS) and RF-MEMS", Sensors and Actuators A: Physical, vol. 272, pp. 187-198, 2018.

[2] V. Gazis, "A survey of standards for machine-to-machine and the internet of things", IEEE Comm. Surv. Tutor, vol.19, pp. 482–511, 2016.

[3] M. Moghavvemi, "Performance Review of High-Quality-Factor, Low-Noise, and Wideband Radio-Frequency LC-VCO for Wireless Communication [Application Notes]",*Microwave Magazine*, vol. 12, pp. 130-146, June 2011.

[4] BehzadRazavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw hill ed., 2002.

[5] A. Hajimiri and T. H. Lee, "Jitter and Phase noise in ring oscillators", *IEEE J. Solid State Circuits*, 34(6):790-804, June 1999.

[6] B. Razavi, *RF Microelectronics*, Prentice-Hall, 1998.

[7] S. Levantino, C. Samori, A. Bonfanti, S.L.J. Gierkink and A.L. Lacaitai, "Frequency dependence on bias

current in 5 GHz CMOS VCOs: impact on tuning range and flicker noise up conversion", IEEE J. of Solid-State Circuits, vol. 37, pp. 1003-1011, Aug. 2002.

[8] MrunaliniNandanwar and Deepak Dandekar, "High Performance VCO for Low Power RF Transmitter-A Review", the National Conference on Innovative Paradigms in Engineering & Technology (NCIPET-2012), pp. 22-25, 2012.

[9] Mohammad Niaboli- Guilani, Dalenda Ben Issa, Abdennaceur Kachouri and Mounir Samet, "A Low Power Low Phase Noise CMOS Voltage Controlled Oscillator",in 17th International Conference Electronics, Circuits, and Systems (ICECS), pp. 422 - 425, Dec. 2010.

[10] Nabil Boughanmi, "High Q-VCO with Low phase noise for Communications applications",in the International, Design and Test of Integrated Systems in Nanoscale Technology, Conference, pp. 370- 373, 2007.

[11] Han-il Lee, Tae-young Choi, SaeedMohammadi and Linda P.B. Katehi, "An Extremely Low Power 2 GHz CMOS LC VCO for Wireless Communication Applications", The European Conference on Wireless Technology, pp. 31-34, Oct. 2005.

[12] Lin Jia, KiatSeng Yeo and ManhAnh Do, "A Novel Methodology for the Design of LC Tank VCO with Low Phase Noise", in IEEE International Symposium on Circuits and Systems (ISCAS), vol. 1, pp 376-379,23-26 May 2005.

[13] Ali Hajimiri and Thomas H. Lee,"Phase Noise in CMOS Differential LC Oscillators", 1998 Symposium onVLSI Circuits-Digest of Technical Papers, pp. 48-51, Jun 1998.

[14] R. Saeidi, N. Masoumi, F. Kalantari and M. S. Oskooei,"Analyzing of Phase Noise in CMOS LC Oscillators" in the 17th International Conference on Microelectronics (ICM), pp. 330-337, Dec. 2005.

[15] Mohd. ShahrulAmran, Queennie Lim SuanImm and Albert Victor Kordeschl, "Design of a 130nm CMOS Differential Cross-coupled 5 GHz LC Oscillator", in proceeding of Asia-Pacific on applied electromagnatics, pp.20-21, December 2005.

[16] Zhou Mingzhu, "A low phase noise wideband VCO in 65nm RF CMOS for low power applications,"in International Conference Microwave and Millimeter Wave Technology (ICMMT), pp. 1 - 4, May 2012

[17] Cheol-Hoe Kim, Soo-Hwan Shin, and Hyung-Joun Yoo,"A Low Phase Noise and Low Power Series Coupled Quadrature VCO Using Reconfigurable LC Tank",in International Conference Radio and Wireless Symposium, pp. 395 - 398, Jan. 2008.

[18] Ali Hajimiri and Thomas H. Lee," Phase Noise in CMOS Differential LC Oscillators", 1998 Symposium on VLSI Circuits-Digest of Technical Papers, pp. 48-51, Jun 1998.

[19] Albert Jerng and Charles G. Sodini, "The Impact of Device Type and Sizing on Phase Noise Mechanisms" ,IEEE journal Of Solid State Circuits, Vol. 40, February 2005.

[20] Sherif Mohamed, MauritsOrtmanns, and YiannosManoli "Design of Current Reuse CMOS LC-VCO", IEEE, 2008.

[21] IjiAyobami B, Forest Zhu, and Michael Heimlich,"Design of Low Power, Wider Tuning Range CMOS Voltage Control Oscillator for Ultra Wideband Applications", IEEE International Conference on IC Design & Technology (ICICDT),pp. 1-4, June 2012.