

Module Current Control and Power Flow Control of Hexagonal Modular Multilevel Converter in Variable Frequency Power System

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Abstract- A transformer-less hexagonal modular multi-level converter (H-MMC) has been introduced for variable frequency regulation in the power generation side. A control algorithm based on the phase-locked loop (PLL) strategy is proposed in this paper to deal with variable frequency on the generation side. Regarding the control to keep balancing the capacitor voltages, the circulating current model is proposed in this paper to control the module current. This research proposes a power flow control strategy considering the current flow between the two sides of the H-MMC. In addition, a modified neutral offset voltage injection method is presented for suppressing the module capacitor voltage by balancing the branch energies.

Keywords- H-MMC, variable frequency regulation, module current control, power flow control

I. INTRODUCTION

Recently, limited fossil resources and environmental issues have been increasingly critical concerns worldwide, resulting in the replacement of renewable energy systems instead of fossil resources-based power plants. In the meantime, Photovoltaic (PV), Wind Turbine (WT) systems have become an essential part of renewable energy systems. But the systems cause voltage differences between distribution feeders. One of the solutions to this problem is to install "power flow controllers" such as static synchronous series capacitors (SSSCs) [1], unified power flow controllers (UPFCs) [2], back-to-back converters (BTBs) [3, 4], and so on.

The BTBs are the most common power converter for reactive power compensation as well as active and reactive power flow control. In SSSC topology, reactive power is injected into the transmission line to control active power flow. However, the SSSC is not able to inject active power. The UPFC consists of series and shunt converters. The series device injects active and reactive power into the transmission line so that the shunt device can take the required active power from the primary or secondary side. However, because of the fractional voltage rating of the

transmission line, the series device in the UPFC may fall into overvoltage under a fault condition. Thus, cascade converter topology, known as a modular multi-level converter (MMC) [5-12], has become an attractive and sustainable solution for the series device in the fault condition. However, multiple dc capacitors should insert instead of transformers. But it is difficult to control the active power flow in the system to maintain the balance of each dc-capacitor voltage.

Hexagonal MMC (H-MMC) is a type of MMC used for three-phase AC-AC conversion, which was first proposed in [13]. Compared with BTB-MMC and modular multi-level matrix converter [14-17], H-MMC consists of only six bridge arms with fewer sub-modules (SMs) and has higher reliability. The H-MMC is suitable for low-frequency energy conversion, and the voltage ripples of the SM capacitors can be reduced by the distortion-less arm currents coupled with two frequency components due to the different frequencies of the two sides of the H-MMC [18]. However, branch currents comprise significant DC components and multiple AC components in H-MMC, which cause an increase in current stress. A circulating current suppression control for H-MMC was proposed to decrease the current stress [19]. H-MMC required a DC

component of the branch current to transfer active power among the ports, and large capacitors were used for DC voltage stability [20], which increases the hardware cost and bulk of equipment. Paper [21] investigated the control of grid-connected H-MMC. However, considering the H-MMC's two sides and the user end, the power flow control has yet to be adopted. Loop current control topology of H-MMC [22, 23] was proposed by the authors in which changing of frequency was directly instructed to the RL load in the case of experimental verification. The control methods differ from this study because of the variable frequencies on both sides of the grid-connected H-MMC.

Therefore, a control algorithm based on the PLL strategy is proposed to deal with variable frequency regulation on the generation side, considering it as the variable frequency system, such as the WT system. This article presents a power flow control strategy based on the output current and the current of each side of the H-MMC. Further, this paper proposes three combined circulating current models: the primary side circulating current control, the secondary side circulating current control, and a loop current control. If the circulating current control is not applied, balancing the power in the system becomes impossible. Regarding the voltage command value, the neutral offset voltage injection method is proposed with the term having the loop current reference, which suppresses the module capacitor voltage by balancing the branch energies. Experimental results validate the feasibility and effectiveness of the proposed control strategies.

II. CIRCUIT CONFIGURATION AND OPERATING PRINCIPLE

Figure 1 depicts the configuration of the grid-connected three-phase H-MMC. Figure 2(a) is the hexagonal circuit configuration of the converter, constructed with six arm modules. Figure 2(b) shows the current flow from one phase to the other of the H-MMC. The currents, such as $i_{rs} = i_r - i_s$ and $i_{vw} = i_v - i_w$ are referred to as the line currents in the H-MMC. Thus, if we pay attention to module A in figure 2(b), the arm current includes both i_{rs} and i_{vw} . Similarly, the arm current for each module processes with the corresponding line-to-line current. A buffer inductor l_b is used in each upper and lower leg of each phase to improve the arm current and prevent the short circuit. Figure 2(c) is the full bridge cell of

the arm module. R, S, T Terminals are the primary side of the power line, and terminals of U, V, W are considered the secondary side.

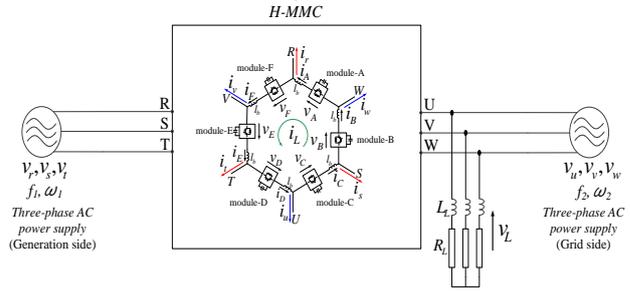


Fig. 1. Grid-connected three-phase H-MMC.

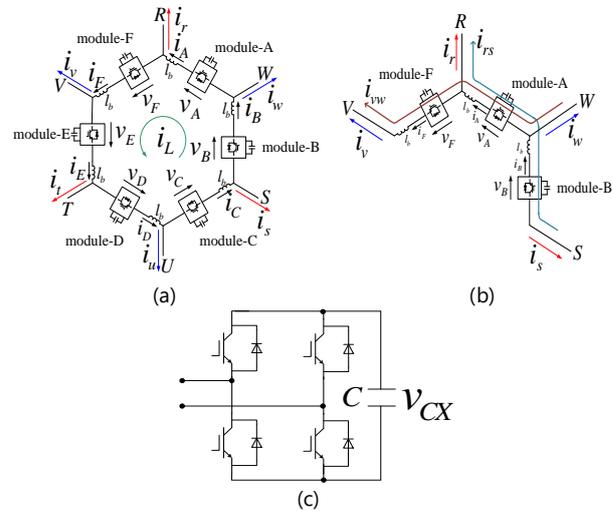


Fig. 2. Hexagonal MMC topology; (a) Configuration of H-MMC, (b) Definition of the current flow from one phase to another of the H-MMC, (c) Configuration of the cell consisting of the two-quadrant chopper.

v_r, v_s, v_t , and i_r, i_s, i_t are the primary side voltage and current, respectively. v_u, v_v, v_w , and i_u, i_v, i_w are the grid side voltage and current, respectively. In the existing system, we have inserted two voltage sensors on each side to detect the line-to-line voltage v_{rs}, v_{st} , and v_{uv}, v_{vw} , respectively. Then v_{tr} and v_{wu} are calculated; these six line-to-line voltages are transformed into phase voltage v_r, v_s, v_t , and v_u, v_v, v_w for each side, respectively. v_{CX} is the corresponding capacitor voltage of the module where $X=A, B, \dots, F$. f_1 is the primary side frequency, and f_2 is the frequency of the secondary side. ω_1 and ω_2 are the angular frequency of each side, respectively. Both sides' power flows to the cells' floating capacitors through R, S, T nodes and U, V, W nodes. Then it is essential to regulate the power flow between two sides and the capacitor voltage in the cells by controlling the output voltage of the modules. $v_A, v_B, v_C, v_D, v_E, v_F$, and $i_A, i_B, i_C, i_D, i_E, i_F$ are each module's voltage and

current in the regular order. R_L and L_L are the load resistors and inductors, respectively. v_L is the output voltage and i_{Lu} , i_{Lv} , i_{Lw} are the output currents.

III. PROPOSED CONTROL STRATEGIES FOR THE THREE-PHASE H-MMC

1. Secondary side power flow control- I_{p2}^* and I_{q2}^* are the current references for the secondary side's active and reactive current components I_{p2} and I_{q2} , respectively. This paper proposes the power flow control strategy by numerically adjusting the grid side active current reference, I_{p2}^* . The reactive current reference I_{q2}^* of the secondary side is set at 0. Figure 3 is the block diagram showing the power flow control on the H-MMC's secondary side. The phase current references i_u^* , i_v^* , and i_w^* are calculated by inversely transforming these pq quantities.

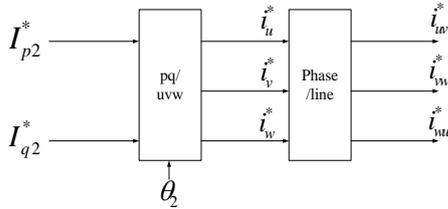


Fig. 3. Block diagram of the H-MMC's secondary side power flow control.

Furthermore, the obtained phase current references are converted into the line-to-line current references i_{uv}^* , i_{vw}^* , and i_{wu}^* . The phase angle θ_2 , obtained by one of the general PLL algorithms, used in the pq inverse transformation is synchronized with the secondary side u -phase. i_{uv}^* , i_{vw}^* , i_{wu}^* are the line-to-line current references of i_{uv} , i_{vw} , i_{wu} , respectively. Thus, arm current control and the power flow control in the H-MMC are obtained by inserting i_{uv}^* , i_{vw}^* , i_{wu}^* to the references of the arm current.

2. Primary side power flow control- Power is supplied from the H-MMC to the secondary side; as discussed in the previous section, deficiency or imbalance occurs in the capacitor voltages of the modules in principle. This section shows how to control the capacitor voltage to a constant value by performing a power flow analysis in each module. The equations below present the primary and grid-side instantaneous voltage and current values. V_1 , I_1 and V_2 , I_2 are of both sides' instantaneous voltage and current amplitude, respectively.

$$v_r = \sqrt{2}V_1 \sin \theta_1, \tag{1}$$

$$i_r = \sqrt{2}I_1 \sin(\theta_1 - \phi_1), \tag{2}$$

$$v_u = \sqrt{2}V_2 \sin \theta_2, \tag{3}$$

$$i_u = \sqrt{2}I_2 \sin(\theta_2 - \phi_2), \tag{4}$$

ϕ_1 is the power factor angle on the primary side (RST node). ϕ_2 is the power factor angle on the grid side (UVW node).

$$P_A = P_C = P_E = \frac{1}{T_1} \int_0^{T_1} v_r i_{rs} dt - \frac{1}{T_2} \int_0^{T_2} v_w i_{vw} dt, \tag{5}$$

$$= \frac{V_1 I_1}{\sqrt{3}} \cos(\phi_1 - \frac{\pi}{6}) - \frac{V_2 I_2}{\sqrt{3}} \cos(\phi_2 - \frac{5}{6} \pi)$$

$$P_B = P_D = P_F = -\frac{1}{T_1} \int_0^{T_1} v_s i_{rs} dt + \frac{1}{T_2} \int_0^{T_2} v_w i_{wu} dt, \tag{6}$$

$$= -\frac{V_1 I_1}{\sqrt{3}} \cos(\phi_1 - \frac{5}{6} \pi) + \frac{V_2 I_2}{\sqrt{3}} \cos(\phi_2 - \frac{\pi}{6})$$

In order to perform the proper operation of the H-MMC, it is a condition that the total capacitor voltage is balanced to a constant value. Since the capacitor voltage depends on the stored power, this condition is satisfied by balancing the periodic average power P_X ($X=A, B, \dots, F$) to a constant value. Here, all the modules' average power P_{ALL} is defined as follows.

$$P_{ALL} = \frac{1}{6} \sum_{X=A}^F P_X \quad (X = A, B, \dots, F), \tag{7}$$

Each module's voltage and current directions are defined in the same direction as shown in figure 2(a); while $P_X > 0$, the module supplies power, and the capacitor voltage drops. On the other hand, while $P_X < 0$, the module receives power, and the capacitor voltage rises. Therefore, the average capacitor voltage of all modules decreases when $P_{ALL} > 0$, and the average voltage increases when $P_{ALL} < 0$, the average capacitor voltage must remain constant.

Thus,

$$P_{ALL} = 0, \tag{8}$$

$$P_{ALL} = \frac{1}{2} \left[\frac{V_1 I_1}{\sqrt{3}} \cos(\phi_1 - \frac{\pi}{6}) - \frac{V_2 I_2}{\sqrt{3}} \cos(\phi_2 - \frac{5}{6} \pi) + \left\{ -\frac{V_1 I_1}{\sqrt{3}} \cos(\phi_1 - \frac{5}{6} \pi) + \frac{V_2 I_2}{\sqrt{3}} \cos(\phi_2 - \frac{\pi}{6}) \right\} \right], \tag{9}$$

$$= \frac{1}{2} (V_1 I_1 \cos \phi_1 + V_2 I_2 \cos \phi_2) = 0$$

Here,

$$\begin{cases} I_{p1} = I_1 \cos \phi_1 \\ I_{p2} = I_2 \cos \phi_2 \end{cases}, \tag{10}$$

$$V_1 I_{p1} + V_2 I_{p2} = 0, \tag{11}$$

Using equations (5) and (6), P_{ALL} becomes as follows by the equations (7) and (8). Then, equation (9) can be rewritten as the equation (11). By satisfying the above equation in the steady state, the average value of the capacitor voltage of all modules can be regulated at a constant value.

Assuming the power is balanced, the power between the input and output can be kept as the active component I_{p1} of the primary side with the active component of the secondary side I_{p2} , as shown in equation (12). The primary side active current command value I_{p1}^* is generated as in equation (13), which includes two terms. The first term is the PI controller, which regulates the average capacitor voltage of all capacitors, V_{C_ave} to the capacitor voltage reference, where $V_{C_ave} = (V_{C_ACE} + V_{C_BDF})/2$. V_{C_ACE} and V_{C_BDF} are obtained as the equation (14). V_C^* is the capacitor voltage command value. The second term is the feed-forward term of the secondary side active current reference, as in equation (12), added in equation (13). Then it is possible to control the average value of all capacitor voltages alongside the primary side current flow control. In the steady state, the PI controller part becomes constant and is a smaller value, equal to the converter's loss. As a result, I_{p1} is very close to I_{p2} . Thus the power between the primary and secondary sides becomes constant.

$$I_{p1} = -\frac{V_2}{V_1} I_{p2} \tag{12}$$

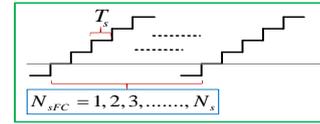
$$I_{p1}^* = \left(K_{PP} + \frac{K_{IP}}{s} \right) (V_{C_ave} - V_C^*) - \frac{V_2}{V_1} I_{p2}^* \tag{13}$$

$$V_{C_ACE} = \frac{V_{CA} + V_{CC} + V_{CE}}{3}; V_{C_BDF} = \frac{V_{CB} + V_{CD} + V_{CF}}{3} \tag{14}$$

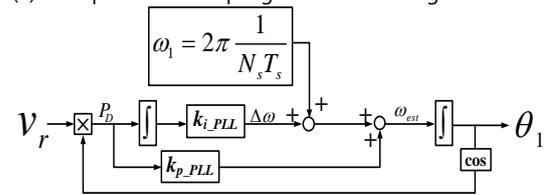
Here, K_{PP} and K_{IP} are the PI controller gains. The reactive current reference I_{q1}^* on the primary side is set to 0 to define the unity power factor on the primary side. The primary side pq references I_{p1}^* and I_{q1}^* , are converted to form the phase current references i_r^* , i_s^* , i_t^* using pq inverse transformation with the phase angle θ_1 obtained by PLL algorithm on the primary side, synchronized with the r -phase. Then the line current references i_{rs}^* , i_{st}^* , i_{tr}^* on the primary side are calculated. i_{rs}^* , i_{st}^* , i_{tr}^* are the line-to-line current references of i_{rs} , i_{st} , i_{tr} , respectively. Then the arm current references are defined using i_{rs}^* , i_{st}^* , i_{tr}^* alongside i_{uv}^* , i_{vw}^* , i_{wu}^* .

In order to verify the stability at the time of transient operation, a method has been proposed to regulate the primary frequency by the modified PLL algorithm

shown in figure 4, where the primary side angular frequency, $\omega_1 = 2\pi/N_s T_s$. N_s and T_s are the sampling count and sampling time in each cycle of v_r . When the frequency of v_r changes, N_s is measured instinctively by the control algorithm and multiplied with T_s to define the primary side frequency f_1 in the control program.



(a) Example of the sampling count of a voltage waveform.



(b) Block diagram of the proposed control method for frequency regulation based on PLL.

Fig. 4. Proposed primary side frequency regulation control.

3. Internal loop current control- In H-MMC, the voltage balance may be lost between modules A, C, E and modules B, D, F. Thus, balancing the voltage during this period leads to balancing the voltage of the entire capacitors. Therefore, an internal loop current can eliminate the voltage imbalance between the modules by accommodating the active power between modules A, C, E and B, D, F. Considering this, the loop current reference i_L^* is designed using the PI controller, expressed in equation (15). While $V_{C_ACE} = V_{C_BDF}$, current i_L^* becomes constant in the steady state. K_{PI} and K_{II} are the gains for adjusting the internal loop current. Regarding the voltage command value, the neutral offset voltage v_L^* injection method is proposed with the term i_L^* as the equation (16) in this study and verified the outcome of the technique.

$$i_L^* = \left(K_{PI} + \frac{K_{II}}{s} \right) (V_{C_BDF} - V_{C_ACE}) \tag{15}$$

$$v_L^* = \left| K_{PV} (V_{C_BDF} - V_{C_ACE}) \right| + K_D i_L^* \tag{16}$$

v_L^* and i_L^* are DC components. v_L^* allows the internal loop current i_L^* to flow, and active power forms by V_{C_ACE} and V_{C_BDF} with i_L^* . K_{PV} and K_D are the gains that adjust the voltage. It is unknown which one of V_{C_ACE} and V_{C_BDF} is larger, so the absolute value uses the amount of error because the direction of v_L^* is fixed. The first term in equation (16) becomes 0 in the steady state. In addition, assuming the internal

resistance of the buffer inductor, a small DC voltage has been added in equation (16), which is proportional to the current i_L^* .

4. H-MMC primary and secondary side circulating current control- In the H-MMC, the target frequencies differ between the Δ -connected MMC seen from the primary side RST terminal and the Δ -connected MMC seen from the secondary side UVW terminal, so the circulating current is divided into the primary side and secondary side. The primary and secondary sides' circulating current command values i_{z1}^* and i_{z2}^* are given by the equations (17) and (19) using the PI control. Deliberately the amplitudes in equations (17) and (19) were changed to regulate the three-phase unbalanced situation and to unbalance the capacitor voltages.

$$i_{z1}^* = -(K_{LP} + K_{LI} \int dt) \begin{bmatrix} v_{C_{ave}} - v_{C_{RS}} & v_{C_{ave}} - v_{C_{ST}} & v_{C_{ave}} - v_{C_{TR}} \\ \sin \theta_1 \\ \sin(\theta_1 - \frac{2}{3}\pi) \\ \sin(\theta_1 + \frac{2}{3}\pi) \end{bmatrix}, \quad (17)$$

$$v_{C_{RS}} = \frac{v_{CA} + v_{CB}}{2}; v_{C_{ST}} = \frac{v_{CC} + v_{CD}}{2}; v_{C_{TR}} = \frac{v_{CE} + v_{CF}}{2}, \quad (18)$$

$$i_{z2}^* = -(K_{LP} + K_{LI} \int dt) \begin{bmatrix} v_{C_{ave}} - v_{C_{UV}} & v_{C_{ave}} - v_{C_{VW}} & v_{C_{ave}} - v_{C_{WU}} \\ \sin \theta_2 \\ \sin(\theta_2 - \frac{2}{3}\pi) \\ \sin(\theta_2 + \frac{2}{3}\pi) \end{bmatrix}, \quad (19)$$

$$v_{C_{UV}} = \frac{v_{CD} + v_{CE}}{2}; v_{C_{VW}} = \frac{v_{CF} + v_{CA}}{2}; v_{C_{WU}} = \frac{v_{CB} + v_{CC}}{2}, \quad (20)$$

The PI controller affects the amplitude of the three-phase current. In the steady state, the current reaches the constant amplitude and balances the three-phase current. K_{LP} and K_{LI} are the PI gains for adjusting the circulation amount. The capacitor voltage can be balanced with the circulating current to form an active power with each line voltage on the primary side.

Equation (21) shows the internal circulating current command value i_l^* of H-MMC, which is the sum of equations (18), (20), and the pure loop current command value, i_L^* from equation (15).

$$i_l^* = i_{z1}^* + i_{z2}^* + i_L^*, \quad (21)$$

5. Arm current control based on internal model principle- The arm current reference i_X^* ($X=A, B, \dots, F$) for each module is given by the equations (22)-(27) using the line-to-line current references and the loop

current reference. This control algorithm allows power conversion with variable voltage and variable frequency.

$$i_A^* = i_{rs}^* + i_{vw}^* + i_l^*, \quad (22)$$

$$i_B^* = i_{rs}^* + i_{wu}^* + i_l^*, \quad (23)$$

$$i_C^* = i_{st}^* + i_{wu}^* + i_l^*, \quad (24)$$

$$i_D^* = i_{st}^* + i_{uv}^* + i_l^*, \quad (25)$$

$$i_E^* = i_{tr}^* + i_{uv}^* + i_l^*, \quad (26)$$

$$i_F^* = i_{tr}^* + i_{vw}^* + i_l^*, \quad (27)$$

The arm current references are superposed signals of sine waves with two frequencies on the primary and secondary sides. If synchronous-coordination transformation and PI control are applied to each arm for such a current command, steady-state deviation and control delay may occur in principle [24]. Therefore, this study proposes a control strategy based on the internal model principle to control the module current without steady-state error for the sine wave reference. Furthermore, the model includes a term known as the damping coefficient ζ , which improves the stability at the transient time. Finally, each module current is controlled by the following arm current controller v_{XI}^* ($X=A, B, \dots, F$) as in equation (28).

$$v_{XI}^* = \left(K_{Pc} + \frac{K_{Ic}}{s} \right) (i_X^* - i_X) + \frac{s\omega_1^2 K_{Sc1}}{s^2 + 2\zeta\omega_1 s + \omega_1^2} (i_X^* - i_X) + \frac{s\omega_2^2 K_{Sc2}}{s^2 + 2\zeta\omega_2 s + \omega_2^2} (i_X^* - i_X), \quad (28)$$

v_{XI}^* includes PI control and the sinusoidal internal model principle of both sides. K_{Pc} and K_{Ic} are the PI gains. K_{Sc1} and K_{Sc2} are the control gains of the current controller. The first term in equation (28) regulates the DC component of the arm current, while the second and third terms regulate the AC component with ω_1 and ω_2 , respectively.

6. Voltage balance control for each cell- So far, how to control the capacitor voltage between modules A to F have been described when each arm module is regarded as an equivalent voltage source. However, compensation for the capacitor voltage balance between the bridge cells inside each module is not considered, and voltage imbalance may occur due to individual differences in the cells. Therefore, the voltage balance between the modules' cells is realized by applying the balance control v_{BX}^* ($X=A, B, \dots, F$).

The mathematical expression of the control strategy for module A is given in equation (29). The balance control gain K_B and i_A are multiplied by the voltage deviation between v_{CA} and R to S node's capacitor voltage $v_{C_{RS}}$, by the voltage deviation between v_{CA} and the V to W node's capacitor voltage $v_{C_{VW}}$. This strategy allows controlling a module capacitor voltage alongside the corresponding and opposite modules' capacitor voltages. i_A is inserted to determine the power flow direction sign. Control methods for other cells are obtained similarly.

$$v_{BA}^* = -K_B i_A \{ (v_{C_{RS}} - v_{CA}) + (v_{C_{VW}} - v_{CA}) \}, \quad (29)$$

7. Final output voltage reference- Regarding the capacitor voltage control, a term v_{XFF} ($X=A, B, \dots, F$) has been added to the control to speed up the response. The topology controls the primary and the secondary sides' fluctuated voltages while any disturbance occurs, allowing the accurate control of arm current. Focussing on module A in figure 3, when $i_A^* - i_A = 0$, the module voltage v_A becomes equal to voltage v_{wr} , where $v_{wr} = v_w - v_r$. The control methods become as follows.

$$v_{AFF} = v_r - v_w, \quad (30)$$

$$v_{BFF} = -v_s + v_w, \quad (31)$$

$$v_{CFF} = v_s - v_u, \quad (32)$$

$$v_{DFF} = -v_t + v_u, \quad (33)$$

$$v_{EFF} = v_t - v_v, \quad (34)$$

$$v_{FFF} = -v_r + v_v, \quad (35)$$

Then the final voltage references v_X^* ($X=A, B, \dots, F$) for each cell is expressed by the equation (36) with the current control v_{XI}^* , balance control v_{BX}^* , the voltage term v_{XFF} , and neural offset voltage v_L^* .

$$v_X^* = (v_{XI}^* + v_{BX}^* + v_{XFF} + v_L^*) / v_{CX}, \quad (36)$$

The voltage corresponding to the modulation factor is performed individually by comparing it with the triangular wave using the PWM control.

IV. EXPERIMENT

A mini-model of the H-MMC connected to the grid has been developed to verify the feasibility of the

proposed control strategies. Figure 5 shows the frequency setting in the primary voltage source to verify the HMMC operation with the proposed control algorithm during transient operation. Experimental circuit parameters are given in Table 1.

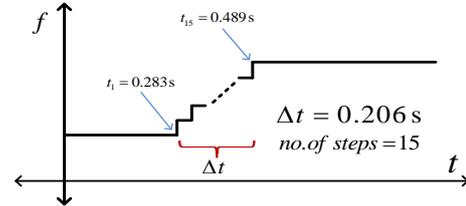


Fig. 5. Determination of frequency in primary voltage source for transient operation.

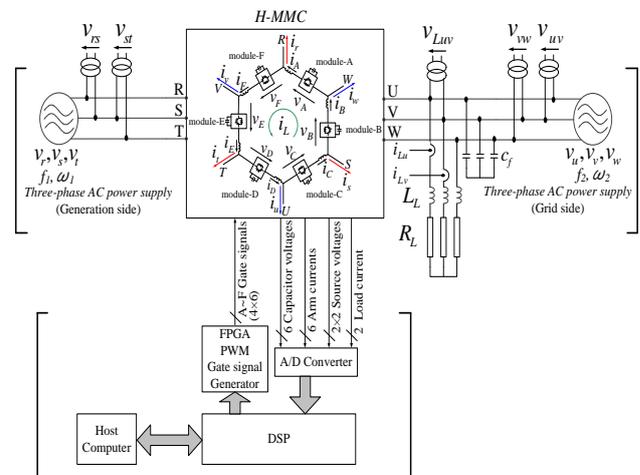


Fig. 6. Experimental configuration of grid-connected three-phase H-MMC.

Table 1 Circuit parameters of the experimental model

Parameter	Value
Primary side Source voltage (v_{rs})	35 V _(L-L)
Secondary side Source voltage (v_{uv})	35 V _(L-L)
Capacitance (C)	4700 uF
Capacitor voltage reference (v_c^*)	70 V
Buffer inductance (l_b)	1.5 mH
Load inductance (L_L)	15 mH
Load resistance (R_L)	25 Ω
Damping coefficient (ζ)	0.01
Active current reference (i_{p2}^*)	1.0 A
Primary side frequency (f_1)	50 Hz
Secondary side frequency (f_2)	60 Hz

Experimental verification of the proposed control strategies for H-MMC has been validated with a sampling time of 250us, and the sampling frequency is 8kHz. Shifted triangular carrier wave and pulse width modulation (PWM) have been executed using

FPGA. Figure 6 shows the experimental system configuration.

Figures 7(a) and 7(c) are the primary and grid side voltage, regulated with 50Hz and 60Hz, respectively. The primary side current shown in figure 7(b) is 2.0A. The secondary side current becomes 1.0A, presented in figure 7(d), as we have set the current reference for the secondary side current $I_{p2}^* = 1.0$.

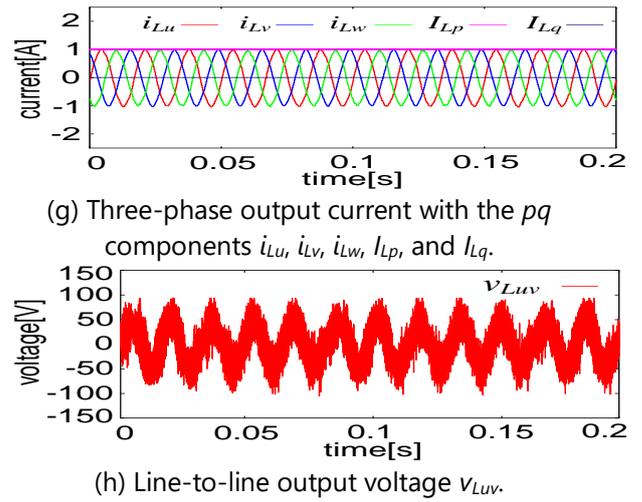
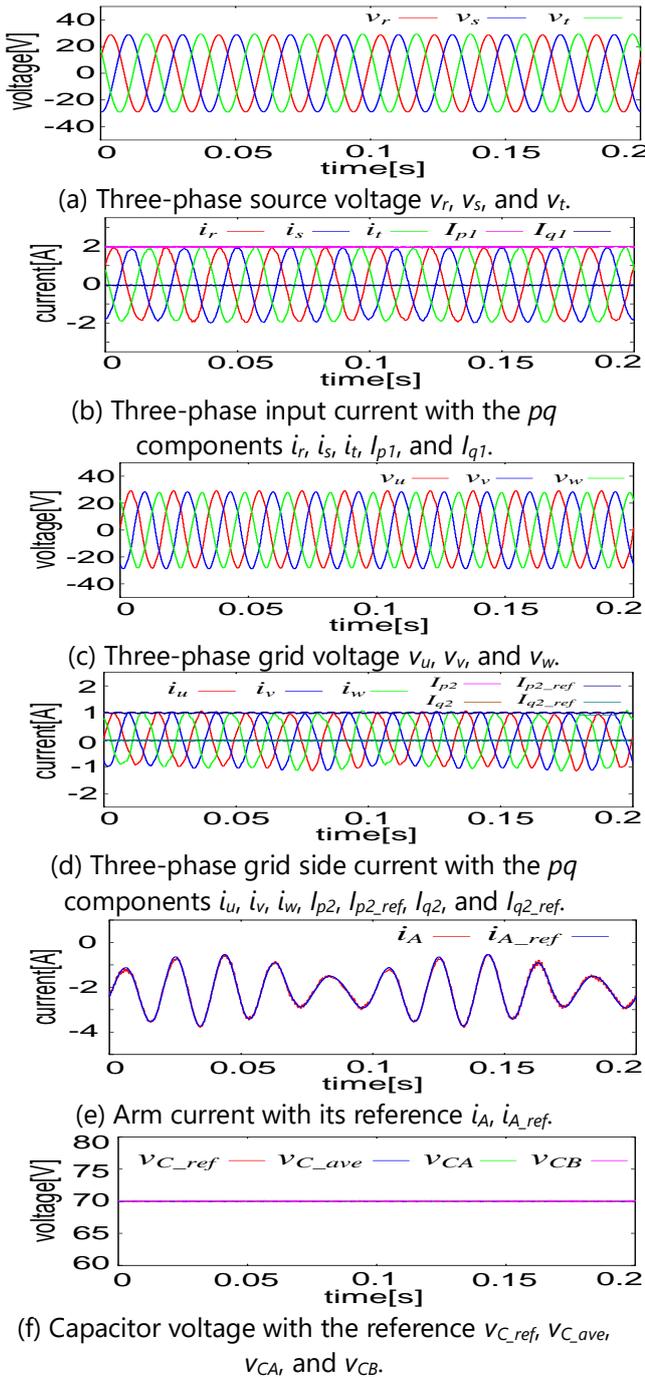


Fig. 7. Experiment results for 50Hz to 60Hz conversion.

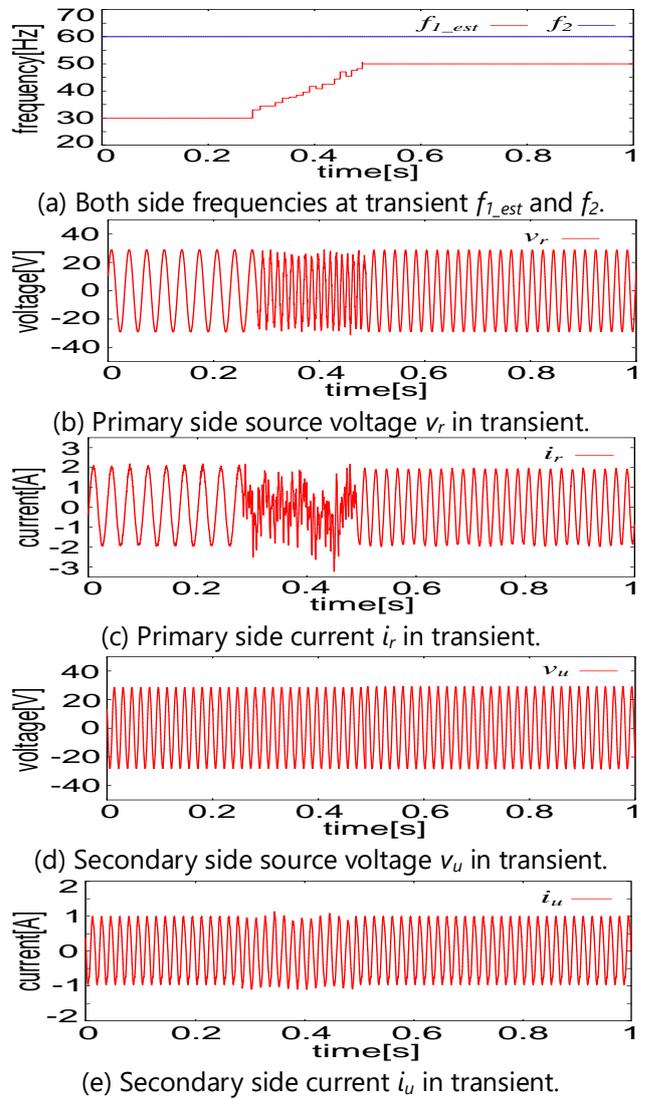


Fig. 8. Transient operation of the H-MMC in which the primary side frequency is regulated between 30Hz and 50Hz.

So the grid side's active and reactive current

references can regulate the secondary side current, as described in figure 3. The pulsation of capacitor voltage has been reduced accordingly by inserting the loop current reference, as in equation (15), into the circulating current reference, given in equation (21). The proposed neutral offset voltage injection method, presented by equation (16) and feed-forward control in equations (30)-(35), suppresses the module voltage fluctuation by balancing the branch energies. As a result, the capacitor voltages shown in figure 7(f) are controlled and regulated within $\pm 0.5V$ with the set capacitor voltage reference at 70V from modules A to F. Since the regulation of the primary side current is obtained with the secondary side current reference, described in equation (13), the capacitor voltages are kept constant at the capacitor voltage reference alongside the balance control by the equation (29).

As in equation (28), by controlling the arm current properly, the deviation has been minimized between the average capacitor voltage of modules A, C, E and the average capacitor voltage of B, D, and F. Looking at the arm current in figure 7(e), it is confirmed that the actual value is followed its command value. From this, it can be seen that the control is operating correctly. The output current with the active component is shown in figure 7(g), having an amplitude of 1.0A. The line-to-line output voltage is shown in figure 7(h).

The experimental verification of the proposed frequency regulation control strategy for the H-MMC has been confirmed by changing the input frequency from 30Hz to 50Hz. The secondary side frequency is fixed at 60Hz. The experimental results for the transient operation are shown in figure 10.

In figure 8(a), the estimated input frequency f_{1_est} ($f_{1_est} = f_1$) has been changed from 30Hz at 0.283s to 50Hz at 0.489s, and the output frequency is fixed at 60Hz. The primary side voltage shown in figure 8(b) is regulated with 30Hz up to 0.283s. Then according to the settings in the primary side power source, the primary frequency has been changed gradually and reached at 50Hz with fifteen steps. Thus the primary side voltage is regulated at 50Hz from 0.49s. In figure 8(c), the primary side current is 2.0A with a frequency 30Hz before the transient but stable at 50Hz from 0.49s after an ignorable transient time within one cycle having the same magnitude from 0.49s. Figure 8(d) is the grid side voltage with the fixed output

frequency, 60Hz. The grid side current is controlled with the current reference, $I^*_{p2} = 1.0$, as shown in figure 8(e). If we pay attention afterward to the transient operation in figure 8(e), the grid side current is unchanged as the time before the step response.

V. CONCLUSION

In this article, the H-MMC is applied to the grid system and proposes how to control power flow on the primary, secondary, and user sides when the frequency change occurs on the primary side, considering it as the WT system. The primary side active current reference includes the control for the average capacitor voltage and a secondary side current reference term. This allows the regulation of the primary side current with the secondary side current reference, and the mean value of the capacitor voltage is controlled as the capacitor voltage reference. Since the accurate control of the arm current is obtained, the capacitor voltages are kept constant at the capacitor voltage reference alongside the proposed three combined circulating current models and the balance control. The neutral offset voltage injection method suppresses the module capacitor voltage fluctuation by balancing the branch energies. Experiment results for the transient case have demonstrated that the proposed control method for the frequency regulation based on PLL for the H-MMC is able to deal with the changed frequency on the generation side and has significant advantages for converting the frequency alongside the power flow control. Since the experimental model of the H-MMC is constructed by one cell in each leg, we will increase the number of cells to deal with the high power.

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