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Design of Area Efficient, Low Power, High Speed 8-Bit Array Multipliers by Using Transmission Gate Logic

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Abstract- The multiplier is the most basic unit of an arithmetic circuit which is predominantly used in digital processing units and several integrated circuits. The efficiency of a processing unit is measured by its speed and power consumption. The multiplier circuit involves an extensive use of adders that generally add to its hardware complexity and thus is a major bottleneck to fast processing and also consumes high power. Thus it becomes critical to improve speed and reduce power consumption in the multiplier module. The conventional multipliers implemented using the CMOS and Transmission Gate (TG) technologies and their combination versions, albeit showing improved speed and low power consumption, still suffer from high hardware complexity. This project proposes the design of an 8-bit Array multiplier. The key idea here is to use the power efficient TG technology based 1-bit hybrid full adder within the popularly used array and Wallace tree multipliers to obtain a new multiplier design with fewer transistors and full output voltage swing. The proposed designs are implemented using Tanner EDA with 90nm technology and simulation results show substantial improvement when compared with the state of the art.

Keywords- Transmission Gate Logic, Conventional CMOS, Pass Transistor Logic, Array Multiplier, Power consumption, propagation delay.

I. INTRODUCTION

Multipliers are predominantly used in microprocessors and digital signal processors and are used extensively for performing arithmetic operations [1]. The modus operandi for multiplication in digital systems is repeated additions of partial products and the conventional multipliers require a large number of adders for partial product addition for higher order multiplication. The most basic multiplier is the array multiplier. Several multiplier circuits have been designed over the years to reduce the number of partial products and also to improve speed, namely the Booth [2], the Wallace tree (WT) [3], the Baugh-Wooley [4] multipliers, etc. These multipliers have been implemented in the conventional complementary metal oxide semiconductor (CMOS). Conventional logic designs like the static CMOS and the pass transistor logic (PTL) are vital in designing full adders in multipliers. The PTL offers advantage in terms of the number of transistors used within the adders.

II. EXISTING TECHNIQUES

1. Conventional CMOS Logic

In conventional or complementary CMOS logic gates are made up of an pmos pull-up and a nmos pull down logic network. CMOS logic style has an

advantage of robustness against voltage scaling and transistor sizing. It has high noise margins and operates reliably at low voltages. Connection of input signals to transistor gates only, facilitates the usage and characterization of logic cells. The complementary transistor pair makes the layout of CMOS gates efficient and straightforward. The major disadvantage of CMOS is substantial number of large PMOS transistors which results in high input loads

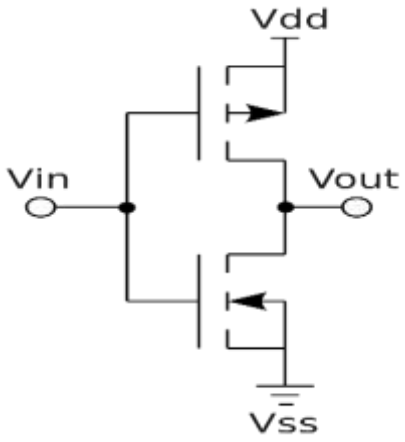

Figure 1: Conventional CMOS Logic

2. Pass Transistor Logic (PTL)

Pass transistor logic (PTL) is a design technique used in Very Large Scale Integration (VLSI) to implement digital logic circuits. Instead of using traditional logic gates like AND, OR, and NOT (which rely on transistors and resistors), pass transistor logic uses transistors to pass logic levels directly between nodes of the circuit. In PTL, MOSFETs (typically NMOS or PMOS transistors) are used as switches to pass or block signals. The source or drain terminals of the transistor are connected to the input or output, and the gate terminal is used to control whether the transistor is on or off. One of the challenges with pass transistor logic is the voltage degradation that can occur. NMOS transistors pass a strong logic '0' but a weak logic '1', while PMOS transistors pass a strong logic '1' but a weak logic '0'. This can introduce logic level issues, which must be managed. PTL circuits can be faster than conventional CMOS circuits because fewer transistors are involved, reducing parasitic capacitance. This leads to faster signal propagation in some cases.

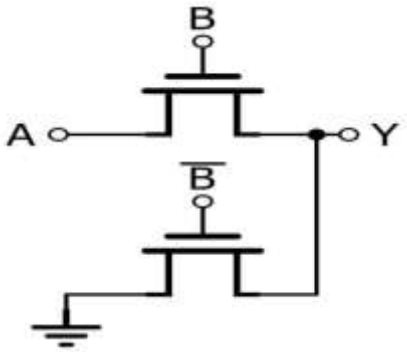

Figure 2: Pass Transistor Logic

III. PROPOSED WORK

1. Transmission Gate Logic (TGL)

Transmission Gate Logic (TGL) is a type of digital logic design that uses CMOS transmission gates to implement logic functions. A transmission gate consists of both an NMOS and a PMOS transistor connected in parallel, controlled by complementary signals. These gates act as electronically controlled switches that allow signals to pass through based on the control input. Transmission gate logic offers several advantages over conventional logic gate implementations, such as reducing transistor count and achieving higher speed, making it a popular choice in certain digital circuit designs, especially for multiplexers, flip-flops, and other switching elements.

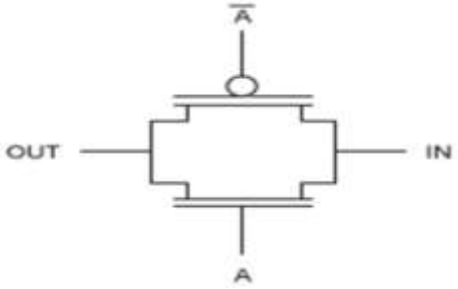

Figure 3: Proposed Transmission Gate Logic Cell

In a transmission gate, both the NMOS and PMOS transistors are controlled in such a way that they complement each other. The NMOS transistor passes a strong logic 0, while the PMOS transistor passes a strong logic 1. By connecting both types of

transistors in parallel, the transmission gate can pass both logic levels effectively. NMOS Transistor: Passes a good logic '0' but suffers voltage degradation when passing a logic '1' (i.e., it doesn't pass a full VDD). PMOS Transistor: Passes a good logic '1' but suffers degradation when passing a logic '0'. When both are combined, the transmission gate can pass both logic levels without any voltage degradation.

2. Array Multiplier

An 8 x 8 array multiplier takes two 8-bit input and generates an output of 16-bits. Let the multiplier and multiplicand be x0 - x7 and y0 - y7 and its outputs are S0- S15. The array multiplication process is shown the figure.

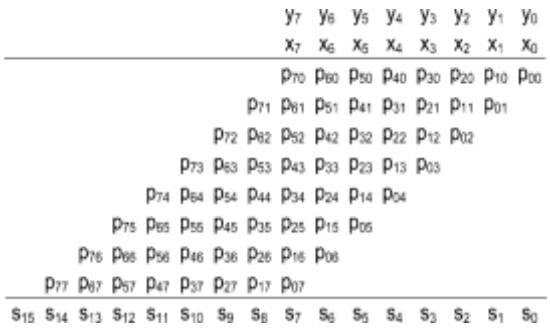

Figure 4. Array Multiplication

In the array multiplier, most of the present inputs for computation of partial sum are depend on the previous output of the adders. Hence, many full adders are idle until the previous output is received from the adders. Hence the delay is more to compute the final product. To reduce the delay of adder, parallel computations of the inputs have to been done in the proposed multiplier. The partial products are added simultaneously and it reduces the number of full adder delays.

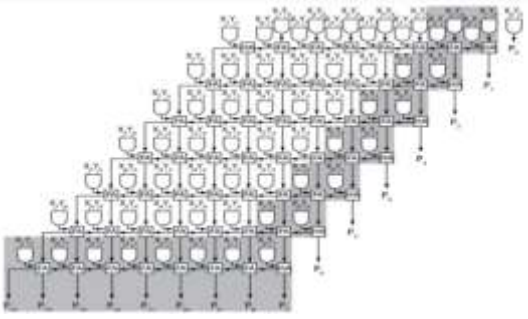
Figure 5: Architecture of 8x8 array multiplier

AND Gates

Used to compute the partial products by multiplying each bit of the multiplicand with each bit of the multiplier. If the multiplicand is x=x7x6x5x4x3x2x1x0 and the multiplier is y=y7y6y5y4y3y2y1y0, then each partial product is obtained by performing the AND operation

Adders (Half and Full Adders)

The partial products are added using Half Adders (HA) and Full Adders (FA). The adders sum up the bits at each level to get the final result. For 8-bit numbers, you'll need 8 rows of adders to handle the summation of the shifted partial products.

Bit Shift

Each row of partial products is shifted to the left (just like decimal multiplication) by one bit for every increase in the position of the multiplier bit.

IV. SIMULATION RESULTS

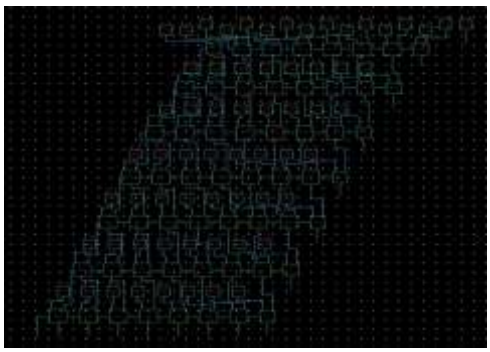
Figure 6: 8x8 Array Multiplier Schematic Diagram


Figure 7: 8x8 Array Multiplier Output Diagram

Table 1: Comparison Table of Different Logics

Parameters	Delay (ps)	Power (mw)	PDP
CMOS based 8x8 Array multiplier	14930	66.05	$0.986x10^{12}$
PTL based 8x8 Array multiplier	3949.3	60.99	$0.240\ x10^{12}$
TGL based 8x8 Array multiplier	3514.1	65.88	$0.231\ x10^{12}$

V. CONCLUSION

The design of an 8-bit array multiplier using transmission gate logic has shown significant improvements in terms of area efficiency, power consumption, and operational speed compared to traditional CMOS-based array multipliers. This approach leverages the advantages of transmission gate logic, which utilizes both nMOS and pMOS transistors in complementary configurations, to achieve lower resistance and reduced switching times. The use of transmission gates minimizes the number of transistors needed for logic operations, resulting in a reduced overall silicon area. This area efficiency is especially beneficial for integrating multipliers in systems with limited space and for applications where high-density design is crucial. Transmission gate logic enables lower static and dynamic power consumption by reducing the number of active switching events and the effective capacitance. This characteristic is particularly beneficial in low-power applications, such as portable and battery-operated devices, where minimizing power usage is essential. Transmission gate logic provides faster transitions due to reduced propagation delays compared to traditional CMOS logic. This enhances the operational speed of the multiplier, making it suitable for high-speed applications that require rapid processing, such as signal processing and real-time data processing systems.

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