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Performance Analogy of Multilevel Inverter with Flipped Sine PWM

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Abstract- Multi-level inverters had the potential of producing better outputs, reduce harmonics in output. They find applications in various fields like motor drives, solar energy systems, and adjustable speed drives. Among different types, cascaded multilevel inverters consists of two DC sources are commonly used in medium to high power needs. This paper compares two control strategies, Sine PWM and flipped Sine PWM, for a cascaded H-Bridge MLI. Inverted/Flipped Sine PWM(ISPWM/FSPWM) technique provides better performance when compared to Sine PWM (SPWM). FSPWM significantly lower the total harmonic distortion (THD) and switching losses compared to traditional SPWM. This paper conducts simulations on three-phase three and five level cascaded H-bridge inverters employing both FSPWM and SPWM control strategies through MATLAB/SIMULINK software.

Keywords- Cascaded H-Bridge Multilevel inverter (CHB MLI), Sine PWM (SPWM), Inverted/Flipped Sine PWM(ISPWM/FSPWM).

I. INTRODUCTION

Multilevel inverters, which generate AC voltage from multiple levels of DC voltage, are increasingly important in medium to large power applications due to their cost-effective solutions. Instead of relying solely on filter size increases, advancements in power electronics and microelectronics focus on increasing number of voltage levels which enhances output magnitude. Compared to two-level inverters, multilevel inverters offer stepped waveforms, resulting in superior quality of power, reduced harmonics, reduced voltage stress, reduced (EMI)electromagnetic interference and enhanced efficiency. Moreover, they had higher power density and voltage-handling capabilities. These inverters play vital roles in various sectors such as renewable energy sources, EV's, industrial sectors, transmitting high-voltage power. The common types of multilevel inverters include neutral-point clamped, capacitor clamped, cascaded H-bridge, offering their own benefits.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER(CHB MLI)

The cascaded MLI, also known as the single phase H- bridge inverter, comprises series-connected H-bridges. In a single-phase cascaded MLI, there are 2(n-1) switches, (n-1)/2 DC sources, and (n-1)/2 H-bridges, where n represents the number of levels.

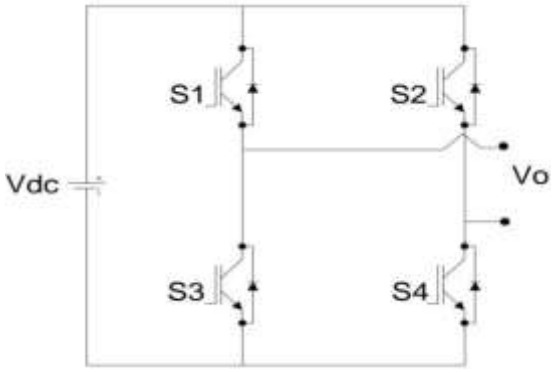


Fig 1: Single phase three-level H-Bridge Multilevel Inverter

Every H- bridge is equipped with individual DC source and generates three distinct levels of voltage. The overall voltage is summation of all DC sources. Considering three-level inverter, overall voltage V= Vdc/2 + Vdc/2 and for five-level, the overall voltage V is summation of Vdc1 Vdc2, where V represents the overall output voltage.

Table-1: Switching sequence of three-level Cascaded H- Bridge inverter

Switching states	Output voltage
S1, S4	Vdc/2
S2, S3	-Vdc/2
S2, S4	0

This three-level inverter comprises 4 switches and one DC source. The three output voltage levels are +Vdc/2, 0, -Vdc/2. Initially, switches 1, 4 are turned on, resulting in the generation of the +Vdc/2 level. Then, switches 2, 3 are activated and generate -Vdc/2.

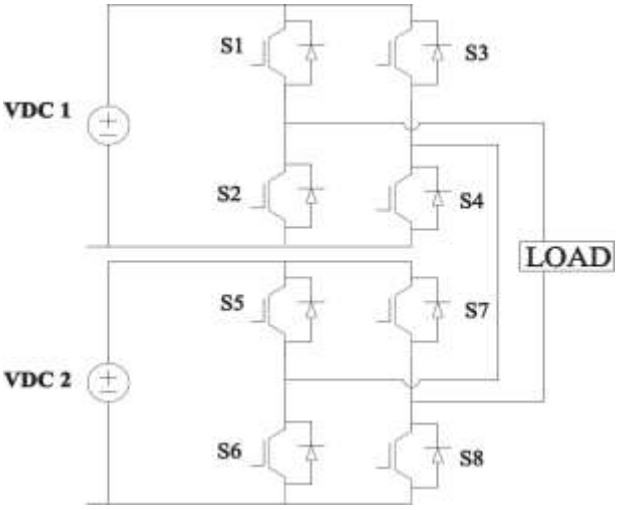


Fig 2: Single phase five-level H-Bridge Multilevel Inverter

Five-level inverter is composed of 8 switches. The five output voltage levels are 0, +Vdc/2, +Vdc, -Vdc/2, and -Vdc. Initially, switches 1, 8, 4 are turned on, allowing only single DC source to conduct, resulting in the generation of the +Vdc/2 level. Then, switches 1, 8, 4, 5 are activated, allowing both DC sources to conduct and generating +Vdc. Subsequently, switches 2, 6, 3 are turned on, utilizing single DC source and causing current to flow in the opposite direction, resulting in the production of -Vdc/2. Finally, switches 2, 6, 7, 3 are activated, enabling both DC sources to conduct with current flowing in the opposite direction, producing -Vdc[1].

Table-2: Sequence of Switching for five-level CHB MLI

S1	S2	S3	S4	S5	S6	S7	S8	Vo
ON	OFF	OFF	ON	ON	OFF	OFF	ON	Vdc
ON	OFF	OFF	ON	OFF	ON	OFF	ON	Vdc/2
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	OFF	ON	OFF	ON	-Vdc/2
OFF	ON	ON	OFF	OFF	ON	ON	OFF	-Vdc

Unlike NPC or FC inverters, cascaded inverters do not necessitate Zener diode or balancing capacitor.

III. SINUSOIDAL PULSE WIDTH MODULATION (SPWM)

Sine PWM is widely used method for converting the voltage DC to AC. It operates by adjusting the square wave's pulse width to synthesize a sine wave with controllable magnitude, frequency.

In this approach, the sine wave is contrasted with triangle waves. If the magnitude of the sine wave exceeds that of the triangle signal, pulses are produced for positive half of the cycle. Conversely, if the magnitude of the triangle wave exceeds than that of the sine wave, pulses are produced for negative half of the cycle[2].

For Sine PWM in Multilevel Inverters, (N-1) carrier signals are utilized for generating N-level outputs. There are two types of carrier-based PWM schemes: 1) Phase Shifted Multi-Carrier Modulation involves shifting phase of multiple carriers. 2) Level Shifted Multi-Carrier Modulation involves shifting the level

of multiple carriers. The second type is further categorized into three types: i) Phase Disposition (PD), ii) Phase Opposition Disposition (POD), and iii) Alternative Phase Opposition Disposition(APOD)[3].

1. Phase Disposition (PD)

Carrier waves which are above and below reference level are synchronized, but their amplitudes are altered.

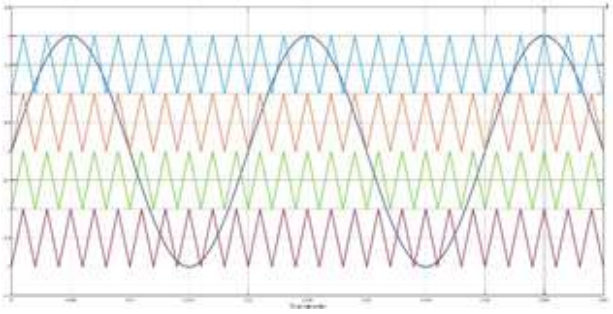


Fig 3: Arrangement of carrier for PD

2. Phase Opposition Disposition (POD)

When the carrier waves above the reference level are synchronized, while the carrier wave below the reference level are in opposite phase, resembling a mirror image when considering the zero level as the mirror.

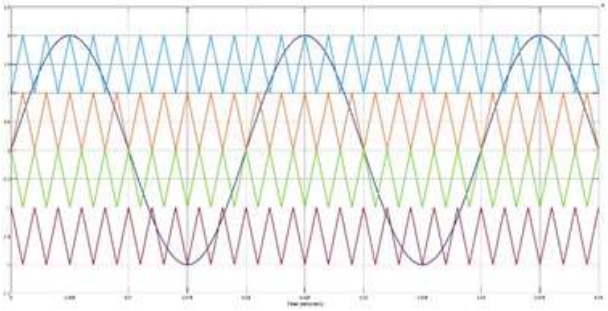


Fig 4: Arrangement of carrier for POD

3. Alternate Phase Opposition Disposition (APOD)

The two neighboring carrier waves are 180 degrees out of phase and resemble mirror images of each other.

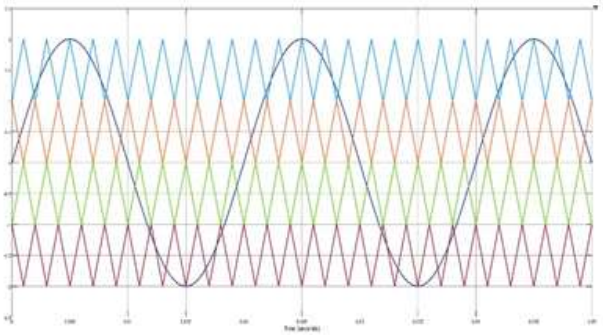


Fig 5: Arrangement of carrier for APOD

IV. FLIPPED SINUSOIDAL PULSE WIDTH MODULATION (FSPWM)

This control strategy utilizes flipped sine waves as carrier signals and sine waves as reference signals. The sine wave contrasted with flipped sine wave, switching signals are generated when sine wave's magnitude exceeds that of the flipped sine wave. The output frequency is determined by the sine wave's frequency, while the switching frequency is defined by the flipped sine wave frequency. This technique typically produces lower THD compared to traditional SPWM [4].

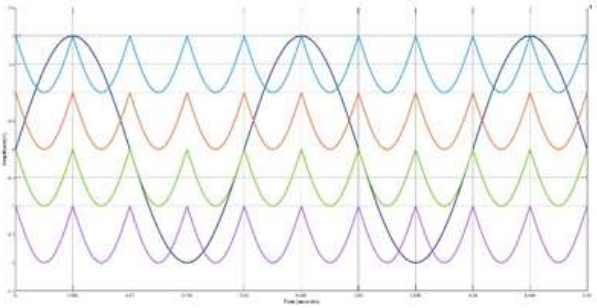


Fig 6: Carrier signals for FSPWM

V. SIMULATION RESULTS AND ANALYSIS

Three phase three-level CHB MLI Simulation

Fig.7 shows simulation circuit of three phase three level H-Bridge MLI employing FSPWM method. Fig.10 represents the respective phase voltages.

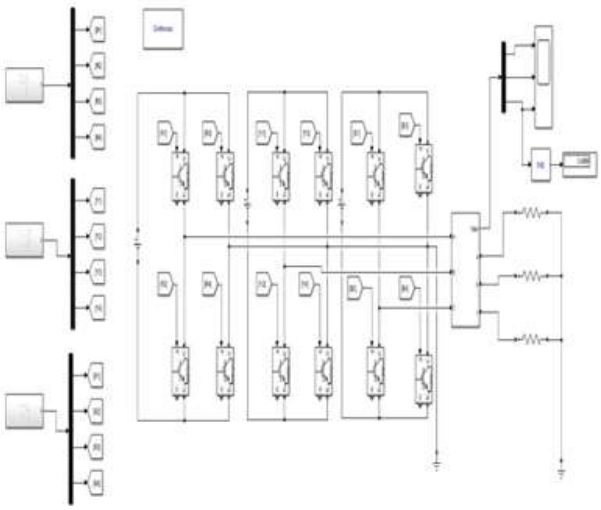


Fig 7: Simulation circuit of three-level cascaded MLI employing FSPWM

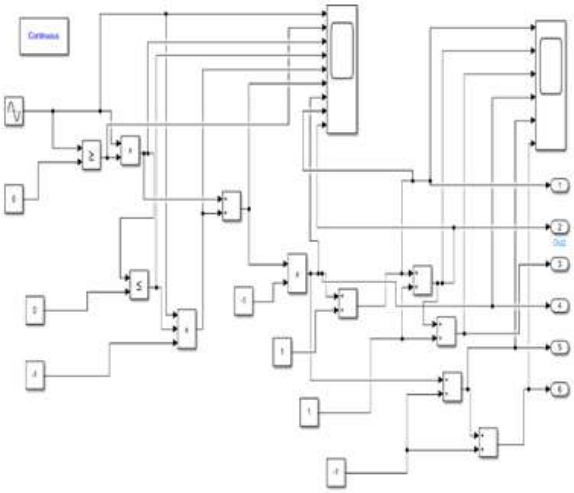


Fig 8: Simulation circuit of FSPWM carrier signals generation

Fig.8 depicts a sub circuit used to generate flipped/inverted sine carrier signals. This circuit generates six flipped sine waves which can be used by seven level inverter. However, for five-level, only four flipped sine pulses are utilized. The reference wave's positive half cycle is contrasted with two of these flipped sine waves and its negative half cycle is contrasted with the remaining two [5].

In Fig.8, the approach involves contrasting sine wave with constant zero. When the sine wave's magnitude exceeds or equals zero, a pulse will be generated, resulting in positive half cycle of sine wave when multiplied together. Next, zero is contrasted with this sine wave's positive half cycle. A pulse is produced when the positive half cycle's magnitude is zero or less [1]. Fig.9 illustrates a carrier signal referred to as the flipped sine signal, which is obtained by multiplying the sine wave by the produced new pulse, constant "-1."

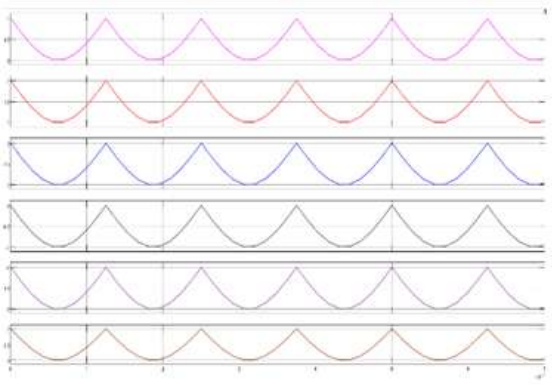


Fig 9: Carrier signals for FSPWM

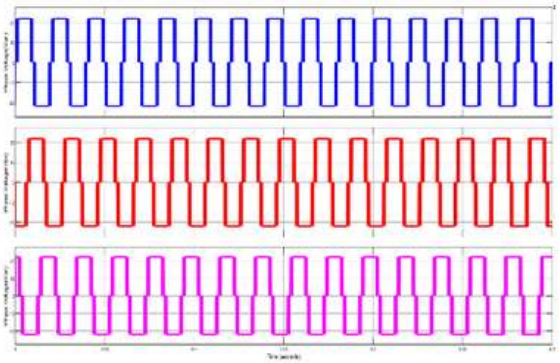


Fig 10: Three-level CHB MLI phase voltages employing FSPWM method

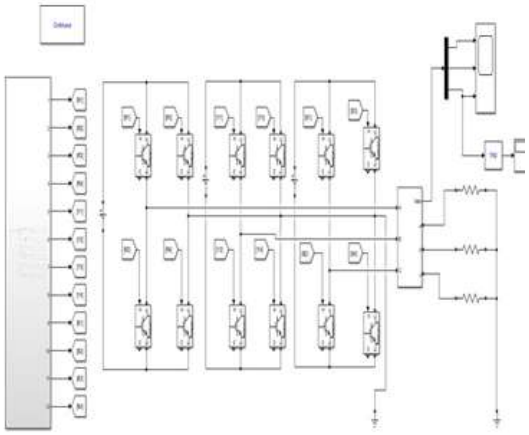


Fig 11: Simulation circuit of three-level H-Bridge MLI employing SPWM method

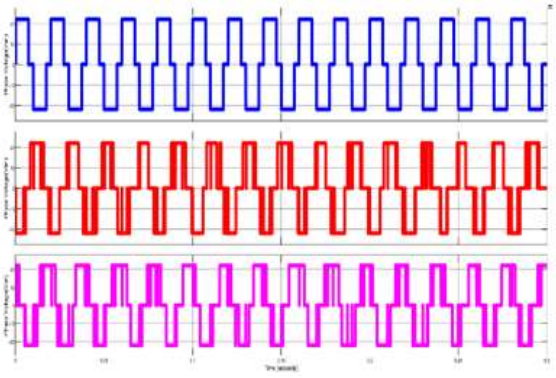
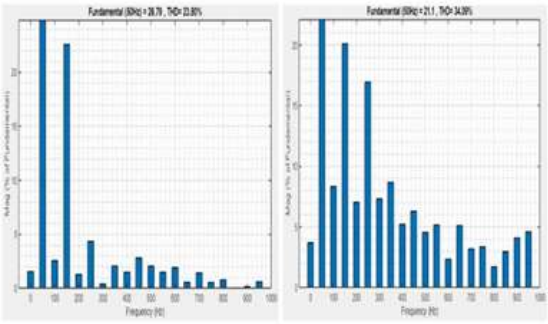


Fig 12: Three-level CHB MLI phase voltages employing SPWM method

Fig.11 shows the simulation circuit of three level H-Bridge MLI employing SPWM method and Fig.12 shows the respective phase voltages.



FSPWM (THD is 23.80%) SPWM (THD is 34.09%)
Fig 13: FFT analogy of FSPWM and SPWM

The FFT Analogy for three-phase three-level cascaded MLI with FSPWM, SPWM is done. It is observed that compared to SPWM the THD is less for FSPWM.

Three phase five level CHB MLI simulation

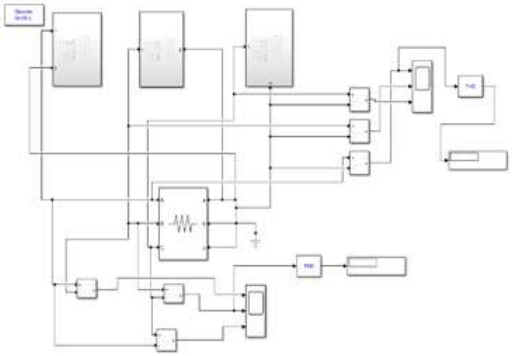


Fig 14: Simulation circuit of five-level H-Bridge MLI employing FSPWM method

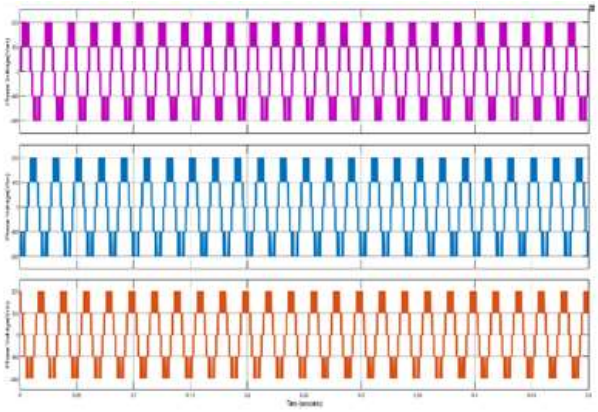


Fig 15: Five-level CHB MLI phase voltages employing FSPWM method

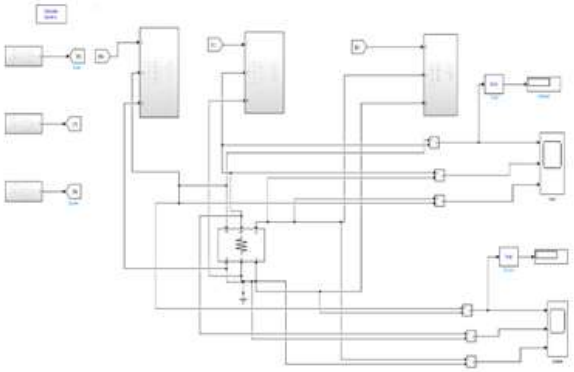


Fig 16: Simulation circuit of five-level CHB MLI employing SPWM method

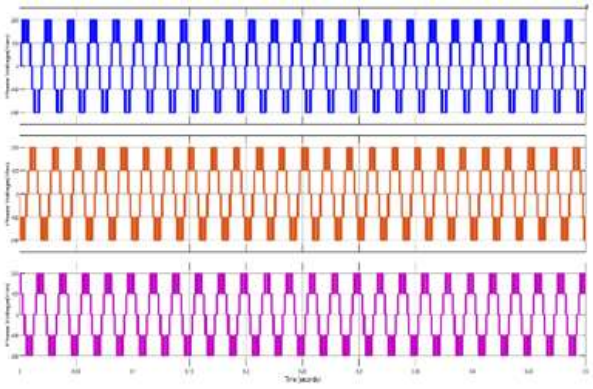
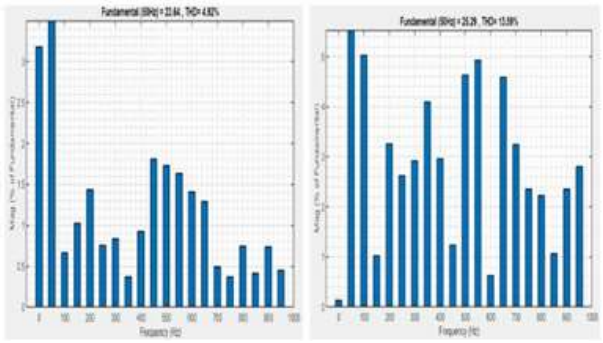


Fig 17: Five-level CHB MLI phase voltages employing SPWM method

Fig.14 and Fig.16 depicts the simulation circuits of five level H-Bridge MLI employing FSPWM and SPWM method and the respective phase voltages employing FSPWM and SPWM are shown in Fig.15 and Fig.17.

Using FFT analogy, THD in the output voltage of a five-level inverter that employing both FSPWM and SPWM is examined.



FSPWM (THD is 4.92%) SPWM (THD is 13.59%)
Fig 18: FFT analogy of FSPWM and SPWM

It is clear from simulation results and FFT analogy that inverters employing FSPWM have lower THD in their output voltage than those using SPWM.

VI. ANALOGY OF TOTAL HARMONIC DISTORTION

THD comparison for three-phase three and five level Cascaded MLI using FSPWM and SPWM is represented in Table-III. Through FFT analogy, we can observe that the THD is lower for five-level CHB MLI compared to three-level. By rising count of levels, THD decreases, output waveform obtained will closely resemble a sinusoidal waveform. FSPWM results in less THD when compared to SPWM.

Table 3: THD analogy employing FSPWM and SPWM methods for Three-Phase Three and Five-level inverters

	FSPWM	SPWM
Three-level	23.80%	34.09%
Five-level	4.92%	13.59%

VII. CONCLUSION

The three and five-level H-Bridge MLI employing flipped sine and SPWM are simulated in MATLAB. The THD for Sine PWM and flipped Sine PWM is contrasted for three phase three and five level CHB MLI using Phase Disposition scheme through FFT analogy. In contrast to SPWM, the harmonics which are obtained for FSPWM are least. The THD for the five level is less contrast to three level and increase in the levels results in lower THD. The conclusion drawn is that the flipped sine PWM method provides enhanced efficiency and performance in contrast to SPWM.

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