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Comprehensive review on VLSI-Based Power-Efficient Booth Multiplier for IoT Applications in FPGA Systems

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Abstract- The rapid expansion of the Internet of Things (IoT) has heightened the need for energy-efficient and high-performance hardware, especially in power-constrained embedded systems. Booth multipliers, widely used for multiplication in IoT applications, are efficient but often consume substantial power. This review paper explores advancements in VLSI-based power-efficient Booth multipliers optimized for FPGA systems in IoT. Focusing on techniques like reduced switching activity, optimized data paths, and minimized signal transitions, the paper highlights innovative designs that achieve lower power consumption while maintaining speed and accuracy. A comparative analysis of power, area, and speed performance metrics demonstrates the effectiveness of these approaches over conventional multipliers. This review provides insights into state-of-the-art power-efficient Booth multipliers, supporting the development of sustainable and high-performance IoT hardware.

Keywords- IoT, VLSI, Booth multiplier, FPGA, low-power design, embedded systems, energy efficiency.

I. INTRODUCTION

The Internet of Things (IoT) is transforming the landscape of technology by connecting everyday devices to the internet, enabling them to collect, exchange, and analyze data. As IoT applications proliferate across various sectors, including healthcare, agriculture, smart cities, and industrial automation, the demand for energy-efficient designs becomes increasingly critical. Many IoT devices are deployed in resource-constrained environments where power supply is limited, such as remote locations or battery-operated systems. Consequently, optimizing power consumption is paramount to prolonging battery life and enhancing the overall sustainability of these devices.

Low-power design not only improves the energy efficiency of IoT devices but also reduces heat generation, which is essential for maintaining system reliability and longevity. Furthermore, regulatory standards and consumer expectations are driving manufacturers to adopt greener technologies, making energy-efficient designs not just a technical necessity but also a market requirement. In this context, the development of specialized hardware architectures that prioritize low power consumption while maintaining high performance is vital.

Multipliers are fundamental components in digital circuits and play a crucial role in various embedded systems, particularly those that involve signal processing, machine learning, and data analysis. They are essential for performing arithmetic operations required in algorithms for tasks such as filtering, modulation, and encryption. In the context of IoT systems, where real-time data processing is often needed, efficient multiplication operations

can significantly impact overall system performance and power efficiency.1.2 Importance of Multiplication in IoT

Multiplication plays a key role in numerous IoT applications, including digital signal processing, cryptography, and machine learning. The computational intensity of multiplication operations necessitates the use of optimized hardware architectures to achieve high performance while minimizing energy consumption. Booth multipliers are commonly used for this purpose due to their ability to reduce the number of partial products, thus enhancing efficiency. However, traditional Booth multipliers often suffer from high power consumption, which can limit their applicability in energy-sensitive environments like IoT.

Challenges in Power-Efficient Design

While Booth multipliers are efficient in terms of reducing the number of partial products, they are prone to significant power consumption, mainly due to high switching activity and signal transitions during operations. In the context of IoT, where devices are often constrained by battery life or low power budgets, traditional multiplier designs fail to meet the power efficiency requirements. This calls for the development of advanced architectures that minimize energy usage while maintaining computational speed and accuracy.

VLSI and FPGA Optimization

Very Large-Scale Integration (VLSI) techniques, when applied to FPGA platforms, provide a promising solution for designing power-efficient Booth multipliers. FPGAs offer flexibility, scalability, and reconfigurability, making them ideal for embedded systems used in IoT applications. By leveraging VLSI techniques such as reducing switching activity, optimizing data paths, and minimizing unnecessary signal transitions, it is possible to achieve significant power savings without compromising performance.

Problem Identification

The need for efficient and high-speed digital processing hardware, especially multipliers, is critical in modern DSP applications. However, current designs and implementations face several limitations:

Limited Bit Width: Most existing Booth multiplier designs are limited to 16-bit implementations, while advanced processors typically operate with 32-bit or higher data widths, creating a performance gap for high-end DSP applications.

Area and Integration Challenges: With ultra-large-scale integration (ULSI) technology, millions of components are integrated on a single chip. However, existing multiplier designs often require larger areas, making them less suitable for efficient ULSI implementation, leading to suboptimal performance in advanced applications.

High Power Consumption: A significant amount of power is consumed by interconnections and off-chip driving, accounting for 20% to 65% of the total power. Current designs exhibit high power consumption, especially in cell library designs, emphasizing the need for further optimization to reduce power usage in ULSI systems. As the demand for portable electronic devices and energy-efficient microelectronics grows, minimizing power dissipation is critical for low-power VLSI circuit design.

Increased Latency: The delay due to clock tree synthesis and total network latency remains a challenge. Current Booth multiplier implementations experience clock delays, which negatively impact response times and overall performance in high-speed applications.

Objective of the Review

This paper provides a comprehensive review of the advancements in VLSI-based Booth multiplier architectures optimized for FPGA systems in IoT applications. The focus is on design strategies and techniques that address power consumption, area utilization, and operational speed. By comparing these innovations to conventional Booth multipliers, the paper aims to highlight the key contributions in the field and explore their potential in the development of sustainable hardware for IoT devices.

II. LITERATURE REVIEW

Booth's algorithm, introduced by Andrew D. Booth in 1951, is a technique for performing multiplication in signed binary numbers, which optimizes the number of addition operations required in multiplication (Booth, 1951). The primary advantage of Booth's algorithm lies in its ability to reduce the number of partial products, thus improving the overall efficiency of multiplication operations. This reduction in complexity is particularly useful in digital systems where resource optimization is crucial, such as in FPGA designs (Chowdhury et al., 2019).

Several adaptations and improvements have been made to Booth's algorithm over the years to enhance its power efficiency and performance in modern hardware. For instance, the Modified Booth Multiplier (MBM) is widely adopted due to its ability to handle both signed and unsigned numbers, reducing computation time by grouping bits and minimizing the number of adders required (Singh & Sharma, 2018). This enhancement has led to its broad application in digital signal processing and arithmetic-intensive tasks.

Low-power design has been a central focus of modern Booth multiplier research, especially in the context of energy-constrained applications such as IoT devices and portable systems. Various design approaches have been developed to reduce power consumption while maintaining performance and area efficiency. A common strategy involves the Modified Booth Encoding (MBE) technique, which reduces the number of partial products to half, significantly lowering dynamic power consumption (Shivashankar et al., 2015).

Another power-efficient approach is Partial Product Reduction using Wallace Tree structures, which reduce the number of logic stages required for product summation. Wallace Tree multipliers are highly effective for reducing propagation delays, making them an ideal choice for high-speed applications, though they typically require more power than other architectures (Chattopadhyay et al., 2017).

Research also highlights the importance of clock-gating techniques, which deactivate portions of the circuit when not in use, significantly reducing switching power in FPGA implementations (Sakthikumaran et al., 2020). Additionally, voltage scaling and operand optimization are leveraged to minimize energy consumption without affecting operational accuracy.

Despite these advancements, existing designs often involve trade-offs between power, performance, and area, with no universal solution that excels in all three aspects. As IoT applications demand ultra-low power designs, newer research is pushing toward more aggressive power-saving techniques such as approximate computing in multipliers (Zhang et al., 2020).

The Internet of Things (IoT) has specific requirements that influence the design of FPGA-based systems, particularly regarding power, scalability, and real-time performance (Gubbi et al., 2013). IoT applications, which often operate in remote or power-constrained environments, require low-power, energy-efficient systems that can run without frequent recharging or maintenance (Li et al., 2018).

FPGAs are increasingly being used for IoT systems due to their reconfigurable nature, which allows designers to update and adapt hardware functions even after deployment (Ali et al., 2017). This flexibility is vital for IoT devices that need to handle a diverse range of tasks, from data acquisition to encryption.

For IoT applications, the latency and speed of the system are equally critical. Real-time processing of sensor data in IoT devices demands low-latency computations, and FPGA-based multipliers, such as Booth multipliers, are favored because they enable high-speed arithmetic operations (Misra et al., 2020). Furthermore, IoT devices need to be lightweight and occupy minimal area to fit into small form factors, making efficient VLSI and FPGA designs crucial for integrating complex systems into compact devices.

Many works focus on Booth multipliers designed to reduce power consumption and optimize efficiency. Several approaches (like Radix-4 Booth encoding, Radix-8, and others) aim to achieve power and area efficiency while introducing trade-offs in accuracy.

S. F. Sultana et al. focused on enhancing the efficiency of Fast Fourier Transform (FFT) implementations by utilizing Booth multipliers. FFTs are integral to many digital signal processing (DSP) applications, and the efficiency of the underlying multipliers can significantly impact system performance. The authors used floating-point representations in their complex Booth multipliers to improve precision and handle a wider range of values, making them suitable for high-performance DSP applications. Floating-point arithmetic, while more complex, provides greater dynamic range and accuracy compared to fixed-point, making it ideal for operations involving complex numbers in FFTs. The core advantage of Booth multipliers, particularly in Radix-4 encoding, is their ability to reduce the number of partial products, thus minimizing the computational burden. This encoding technique directly leads to reductions in both area and delay, crucial factors for optimizing hardware implementations. Their FPGA-based implementation, tested on Spartan boards, demonstrated notable improvements in delay and area, showcasing how optimized Booth multipliers can enhance real-time DSP operations such as audio processing and communications.

S. Venkatachalam et al. introduced modified Booth algorithms aimed at reducing both power consumption and area in multiplier designs while incorporating an error-tolerant mechanism. The idea behind error tolerance is to allow slight inaccuracies in the multiplication results in exchange for significant power and area savings. This is particularly useful in applications where exact precision is not critical, such as in multimedia processing or image compression, where minor errors may not impact the final outcome significantly. By modifying the traditional Booth algorithm, the authors achieved a design that consumes less power by reducing the switching activities and number of partial products generated during the multiplication process. Furthermore, their design effectively minimizes the hardware area required, which is essential for resource-constrained systems like Internet of Things (IoT) devices. The trade-off between accuracy and power/area efficiency is a key highlight of this work, as it opens up possibilities for energy-efficient computing in applications where absolute precision can be relaxed.

P. Yin et al. concentrated on developing floating-point Booth multipliers with a focus on optimizing power consumption and reducing delay. Floating-point arithmetic, though more resource-intensive, is essential for applications requiring high precision and dynamic range, such as scientific computing and signal processing. In their study, they employed Booth encoding, particularly Radix-8, which further reduces the number of partial products, thereby minimizing the computational load. The use of Radix-8 encoding compared to Radix-4 significantly cuts down on the number of stages required for multiplication, leading to improved performance in terms of speed and delay. By optimizing the multiplier's architecture for floating-point operations, P. Yin et al. managed to achieve substantial power savings, which is particularly important in energy-constrained environments such as IoT and embedded systems. Their work demonstrates that Booth multipliers can be efficiently adapted for floating-point operations, achieving both power and delay reductions, making them suitable for high-speed, low-power applications.

P. J. Edavoor et al. explored the application of Booth multipliers in multimedia systems, where there is often a need to balance performance and precision. In multimedia processing, such as video and image compression, exact precision is not always necessary. By slightly compromising on accuracy, significant improvements in speed and power efficiency can be achieved. The authors analyzed how Booth multipliers can be optimized to meet these requirements by reducing the number of partial products and using techniques such as Radix-4 encoding to minimize computation overhead. Their work shows that Booth multipliers are particularly well-suited for multimedia

applications because of their ability to process large data sets quickly while maintaining an acceptable level of accuracy, making them ideal for real-time processing scenarios where both speed and efficiency are critical.

V. An et al. focused on the use of Booth arithmetic in Digital Signal Processing (DSP) applications, where reducing errors while maintaining high performance is paramount. In their work, they analyzed various error-tolerant techniques within Booth multiplier designs, particularly for DSP systems that rely on high-speed arithmetic operations like filtering, modulation, and demodulation. The authors discussed the impact of Radix-8 encoding in reducing errors, emphasizing that DSP systems can tolerate small inaccuracies without significantly affecting the overall quality of output. By incorporating error correction mechanisms alongside Booth arithmetic, they achieved improved accuracy while still benefiting from the efficiency gains of Booth encoding. Their design showcases the practicality of Booth multipliers in DSP applications, where performance often outweighs the need for perfect accuracy.

III. GAPS IN EXISTING RESEARCH

The review of Booth multiplier literature highlights several research gaps that remain unexplored. While significant advancements have been made in power efficiency and error tolerance, there is limited exploration of adaptive multipliers that can dynamically adjust precision and power based on real-time system demands, especially in the context of IoT and FPGA-based systems. Additionally, although various hybrid approaches like Booth-Wallace multipliers show potential, further research is needed to optimize their integration with emerging AI and machine learning hardware platforms. The existing work also lacks comprehensive analysis on the impact of advanced process technologies (such as FinFET or GAAFET) on Booth multiplier performance, particularly in ultra-low-power applications. Lastly, more in-depth investigations into energy-efficient designs for high-speed, high-resolution image and video processing, beyond just multimedia applications, could broaden the scope of Booth multipliers' use in evolving computational paradigms.

IV. PROPOSED METHODOLOGY

The proposed research aims to design and implement a high-performance 64x64 bit Booth multiplier. The entire design process will follow a structured flow, as outlined in the flowchart (to be provided), detailing each block of the multiplier design. Below is a breakdown of the specific objectives and steps involved in this work:

Objective: The goal is to implement a 64x64 bit Booth multiplier that improves upon existing designs in terms of speed, power efficiency, and overall performance. This implementation will be specifically targeted at applications in advanced digital signal processing.

Design and Implementation: The Booth multiplier will be designed using Verilog hardware description language. The implementation will be carried out on the Xilinx platform, a popular tool for FPGA-based design, allowing for precise control and optimization of the multiplier's operation.

Parameter Calculation: Key performance metrics will be calculated and analyzed, including:
Area: The physical size occupied by the multiplier on the chip.

- **Power:** The power consumption of the design, critical for power-sensitive applications.
- **Delay:** The time taken for the multiplier to complete its operations, a crucial factor in high-speed DSP applications.
- **Power Delay Product (PDP):** A metric that combines power and delay to assess overall efficiency.
- **Comparison with Existing Multipliers:** The performance of the proposed 64-bit Booth multiplier will be compared with existing implementations. the comparison will focus on improvements in speed, area, power consumption, and the PDP to highlight the advantages of the new design over conventional multipliers.

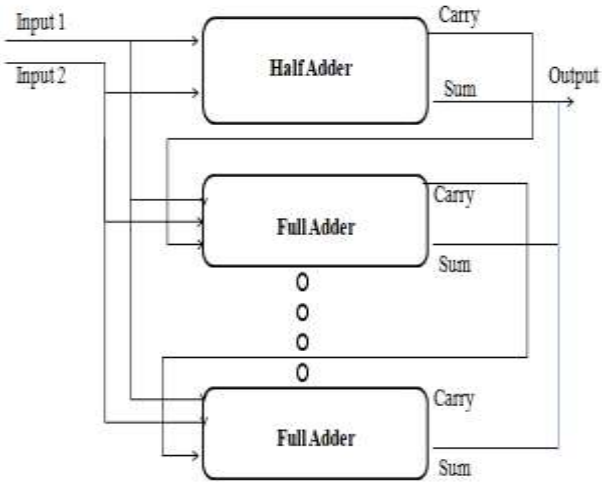

Figure 1 Methodology flow chart

The methodology block diagram illustrates the design of the 64x64 bit Booth multiplier. This design incorporates a combination of half adders and full adders, utilizing one half adder and 63 full adders in total. The multiplier operates using partial product generation, following the principles of a Dadda multiplier. A carry-save adder (CSA) is employed in the process, which is a type of digital adder specifically designed to compute the sum of three or more binary numbers efficiently. Unlike conventional adders, the CSA generates multiple outputs, which are then summed to obtain the final result. The proposed multiplier demonstrates a substantial reduction in error rates, largely attributed to the use of a compressor within the design.

The proposed methodology focuses on the hardware-level implementation of the 64-bit Booth multiplier, emphasizing the key components involved in the design of the multiplier, particularly adders and multipliers commonly used in digital signal processing applications. The implementation process consists of three main stages:

Partial Product Generation: The first step involves generating partial products by performing bitwise AND operations between each bit of one operand and each bit of the other operand. This results in a total of N2N^2N2 partial products, where NNN represents the number of bits in each operand. The organization of the bits influences the carrying process in subsequent steps.

Reduction of Partial Products: In the second stage, the number of partial products is reduced using a hierarchical structure of full and half adders. This stage effectively consolidates the partial products into a manageable number, facilitating efficient computation.

Final Summation: The final step involves aggregating the results of the reduced partial products using a conventional adder. This stage combines the outputs from the previous stage to produce the final multiplication result.

V. CONCLUSION

The literature on Booth multipliers reveals significant advancements in power efficiency, error tolerance, and algorithmic innovations, particularly for applications like digital signal processing (DSP) and multimedia. Power-efficient designs, such as Radix-4 and Radix-8 Booth encodings, focus on reducing power consumption and optimizing area performance, while error-tolerant systems trade slight accuracy losses for substantial gains in speed and energy efficiency. Algorithmic enhancements, like operand rounding and novel transistor-level designs, improve power-delay products, and hybrid approaches, such as Booth-Wallace multipliers, further enhance the balance between power, area, and accuracy. FPGA and ASIC implementations demonstrate the practical viability of these designs, particularly in image processing and real-time applications, where accuracy-performance trade-offs allow for adaptable, power-scaled solutions. Overall, Booth multiplier research continues to push the boundaries of efficiency and flexibility in hardware design.

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