Ms. Mansi Yadav, 2025, 13:1
ISSN (Online): 2348-4098
ISSN (Print): 2395-4752

International Journal of Science, Engineering and Technology

An Open Access Journal

VLSI-Based Power-Efficient Booth Multiplier for IoT Applications in FPGA Systems

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Abstract- As the Internet of Things (IoT) continues to expand, the need for energy-efficient and high-performance hardware becomes critical, particularly for embedded systems where power and resource constraints are paramount. Multiplication is a fundamental operation in many IoT applications, and traditional Booth multipliers, while efficient in reducing the number of partial products, often consume significant power. This research addresses this challenge by proposing a VLSI-based power-efficient Booth multiplier specifically optimized for FPGA systems utilized in IoT applications. The proposed design implements advanced techniques to minimize power consumption without sacrificing computational speed or accuracy. Key optimizations include reducing switching activity, improving data path efficiency, and minimizing unnecessary signal transitions, resulting in a significant reduction in overall energy usage. The architecture is synthesized and implemented on FPGA platforms, ensuring flexibility, scalability, and compatibility with IoT hardware constraints. Performance metrics such as power consumption, area utilization, and operating speed are analyzed and compared to conventional Booth multipliers and other low-power designs. The results demonstrate that the proposed design achieves a significant reduction in power consumption while maintaining high throughput, making it a suitable solution for power-sensitive IoT environments where energy efficiency is critical. This research contributes to the development of more sustainable and high-performance hardware architectures for the next generation of IoT devices.

Keywords- IoT, VLSI, Booth multiplier, FPGA, power-efficient design, low-power architecture, embedded systems, energy efficiency.

I. INTRODUCTION

The Internet of Things (IoT) is transforming the landscape of technology by connecting everyday devices to the internet, enabling them to collect, exchange, and analyze data. As IoT applications proliferate across various sectors, including healthcare, agriculture, smart cities, and industrial automation, the demand for energy-efficient designs becomes increasingly critical. Many IoT devices are deployed in resource-constrained environments where power supply is limited, such as remote locations or battery-operated systems. Consequently, optimizing power consumption is paramount to prolonging battery life and enhancing the overall sustainability of these devices.

Low-power design not only improves the energy efficiency of IoT devices but also reduces heat generation, which is essential for maintaining system reliability and longevity. Furthermore, regulatory standards and consumer expectations are driving manufacturers to adopt greener

technologies, making energy-efficient designs not just a technical necessity but also a market requirement. In this context, the development of specialized hardware architectures that prioritize low power consumption while maintaining high performance is vital.

Multipliers are fundamental components in digital circuits and play a crucial role in various embedded systems, particularly those that involve signal processing, machine learning, and data analysis. They are essential for performing arithmetic operations required in algorithms for tasks such as filtering, modulation, and encryption. In the context of IoT systems, where real-time data processing is often needed, efficient multiplication operations can significantly impact overall system performance and power efficiency.

Importance of Multiplication in IoT

Multiplication plays a key role in numerous IoT applications, including digital signal processing, cryptography, and machine learning. The computational intensity of multiplication operations necessitates the use of optimized hardware architectures to achieve high performance while minimizing energy consumption. Booth multipliers are commonly used for this purpose due to their ability to reduce the number of partial products, thus enhancing efficiency. However, traditional Booth multipliers often suffer from high power consumption, which can limit their applicability in energy-sensitive environments like IoT.

Challenges in Power-Efficient Design

While Booth multipliers are efficient in terms of reducing the number of partial products, they are prone to significant power consumption, mainly due to high switching activity and signal transitions during operations. In the context of IoT, where devices are often constrained by battery life or low power budgets, traditional multiplier designs fail to meet the power efficiency requirements. This calls for the development of advanced architectures that minimize energy usage while maintaining computational speed and accuracy.

VLSI and FPGA Optimization

Very Large-Scale Integration (VLSI) techniques, when applied to FPGA platforms, provide a promising solution for designing power-efficient Booth multipliers. FPGAs offer flexibility, scalability, and reconfigurability, making them ideal for embedded systems used in IoT applications. By leveraging VLSI techniques such as reducing switching activity, optimizing data paths, and minimizing unnecessary signal transitions, it is possible to achieve significant power savings without compromising performance.

Problem Identification

The need for efficient and high-speed digital processing hardware, especially multipliers, is critical in modern DSP applications. However, current designs and implementations face several limitations:

Limited Bit Width: Most existing Booth multiplier designs are limited to 16-bit implementations, while advanced processors typically operate with 32-bit or higher data widths, creating a performance gap for high-end DSP applications.

Area and Integration Challenges: With ultra-large-scale integration (ULSI) technology, millions of components are integrated on a single chip. However, existing multiplier designs often require larger areas, making them less suitable for efficient ULSI implementation, leading to suboptimal performance in advanced applications.

High Power Consumption: A significant amount of power is consumed by interconnections and off-chip driving, accounting for 20% to 65% of the total power. Current designs exhibit high power consumption, especially in cell library designs, emphasizing the need for further optimization to reduce power usage in ULSI systems. As the demand for portable electronic devices and energy-efficient microelectronics grows, minimizing power dissipation is critical for low-power VLSI circuit design.

Increased Latency: The delay due to clock tree synthesis and total network latency remains a

challenge. Current Booth multiplier implementations experience clock delays, which negatively impact response times and overall performance in high-speed applications.

II. RESEARCH OBJECTIVE

The primary goal of this research is to develop a high-speed, low-latency Booth multiplier optimized for advanced DSP applications. Previous designs have primarily focused on 16-bit implementations. To meet the growing demands of modern processors, this research aims to design a 64-bit Booth multiplier using Verilog coding on the Xilinx platform. The project will focus on evaluating key performance metrics such as area, power consumption, delay, and power-delay product (PDP). The aim is to improve current designs to make them suitable for ultra-large-scale integration while reducing power consumption and enhancing performance in DSP systems.

III. PROPOSED METHODOLOGY

The proposed research aims to design and implement a high-performance 64x64 bit Booth multiplier. The entire design process will follow a structured flow, as outlined in the flowchart (to be provided), detailing each block of the multiplier design. Below is a breakdown of the specific objectives and steps involved in this work:

Objective: The goal is to implement a 64x64 bit Booth multiplier that improves upon existing designs in terms of speed, power efficiency, and overall performance. This implementation will be specifically targeted at applications in advanced digital signal processing.

Design and Implementation: The Booth multiplier will be designed using Verilog hardware description language. The implementation will be carried out on the Xilinx platform, a popular tool for FPGA-based design, allowing for precise control and optimization of the multiplier's operation.

Parameter Calculation: Key performance metrics will be calculated and analyzed, including:

- **Area:** The physical size occupied by the multiplier on the chip.
- **Power:** The power consumption of the design, critical for power-sensitive applications.
- **Delay:** The time taken for the multiplier to complete its operations, a crucial factor in high-speed DSP applications.
- **Power Delay Product (PDP):** A metric that combines power and delay to assess overall efficiency.
- **Comparison with Existing Multipliers:** The performance of the proposed 64-bit Booth multiplier will be compared with existing implementations. the comparison will focus on improvements in speed, area, power consumption, and the PDP to highlight the advantages of the new design over conventional multipliers.

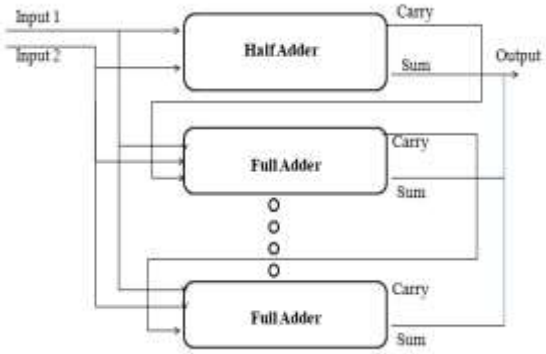

Figure 1 Methodology flow chart

The methodology block diagram illustrates the design of the 64x64 bit Booth multiplier. This design incorporates a combination of half adders and full adders, utilizing one half adder and 63 full adders in total. The multiplier operates using partial product generation, following the principles of a Dadda multiplier. A carry-save adder (CSA) is employed in the process, which is a type of digital adder specifically designed to compute the sum of three or more binary numbers efficiently. Unlike conventional adders, the CSA generates multiple outputs, which are then summed to obtain the final result. The proposed multiplier demonstrates a substantial reduction in error rates, largely attributed to the use of a compressor within the design.

The proposed methodology focuses on the hardware-level implementation of the 64-bit Booth multiplier, emphasizing the key components involved in the design of the multiplier, particularly adders and multipliers commonly used in digital signal processing applications. The implementation process consists of three main stages:

Partial Product Generation: The first step involves generating partial products by performing bitwise AND operations between each bit of one operand and each bit of the other operand. This results in a total of N2N^2N2 partial products, where NNN represents the number of bits in each operand. The organization of the bits influences the carrying process in subsequent steps.

Reduction of Partial Products: In the second stage, the number of partial products is reduced using a hierarchical structure of full and half adders. This stage effectively consolidates the partial products into a manageable number, facilitating efficient computation.

Final Summation: The final step involves aggregating the results of the reduced partial products using a conventional adder. This stage combines the outputs from the previous stage to produce the final multiplication result.

IV. SIMULATION

1. Simulation in XILINX Test Bench

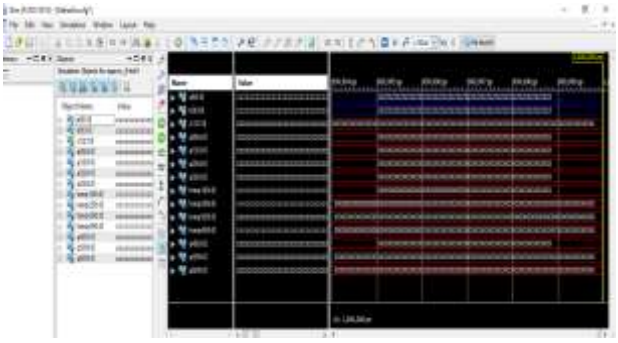

Figure 2 High Impedance.

Figure 2 is showing input and output at Z symbol, it represents the high impedance.

Remaining sub-module or internal signal shows by X.

Figure 3 Blank Space Means

Figure 3 is showing input values of 'a', here binary number 1 shows the active signal and 0 shows the blank space means.

Figure 4 Values of input 'b'

Figure 4 is showing input values of 'b', here binary number 1 shows the active signal and 0 shows the blank space means.

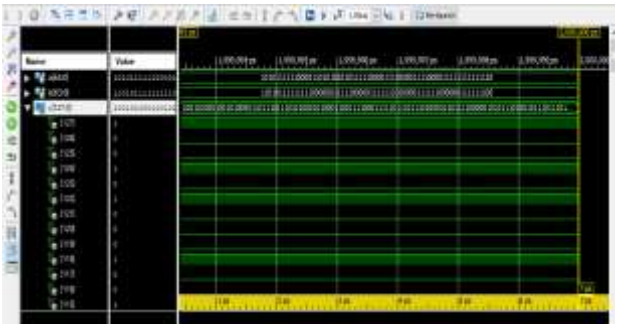

Figure 5 Values of output 'c'

Figure 5 is showing input values of 'c', here binary number 1 shows the active signal and 0 shows the blank space means.

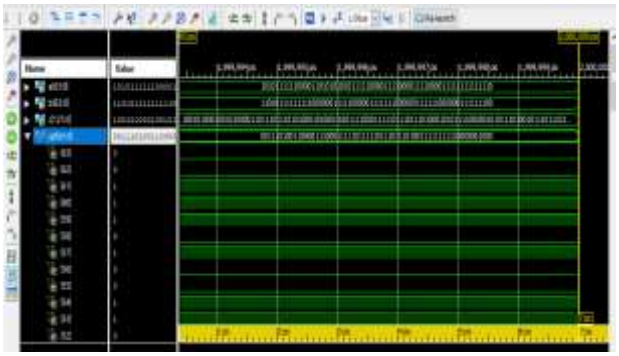

Figure 6 Values of internal signal q0

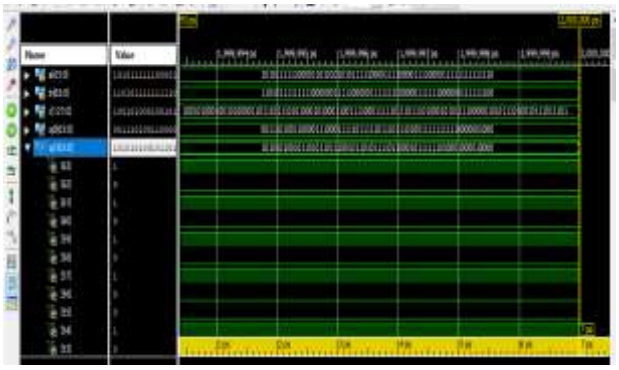

Figure 7 Values of internal signal q1

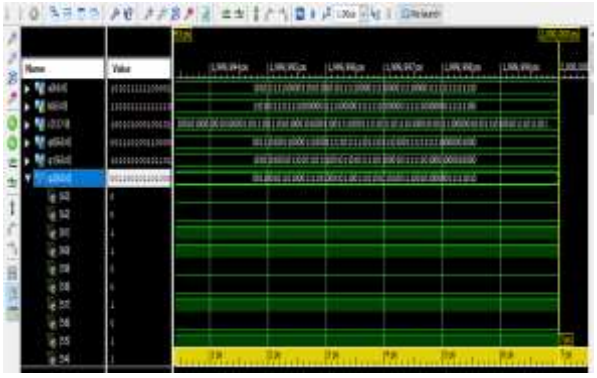

Figure 8 Values of internal signal q2

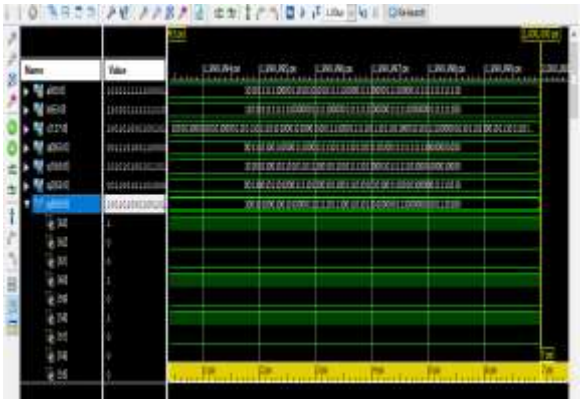

Figure 9 Values of internal signal q3

Figure 6. 7, 8 and 9 are showing internal signal q0, q1, q2 and q3 signals.

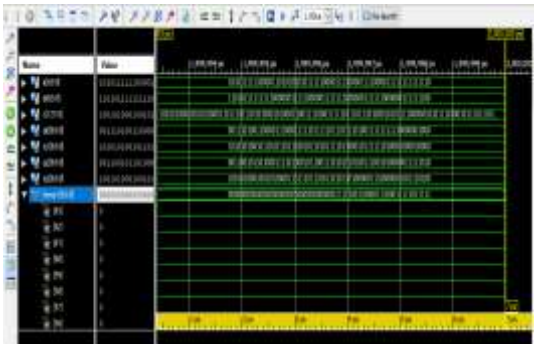

Figure 10 Values of internal signal temp1

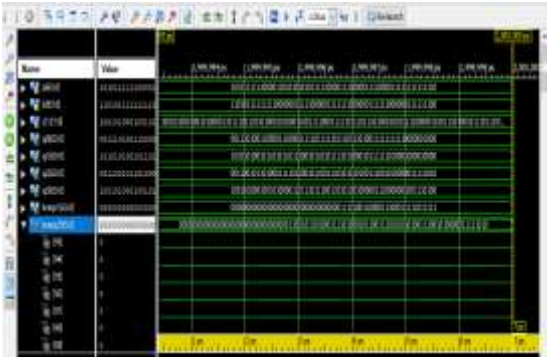

Figure 11 Values of internal signal temp2

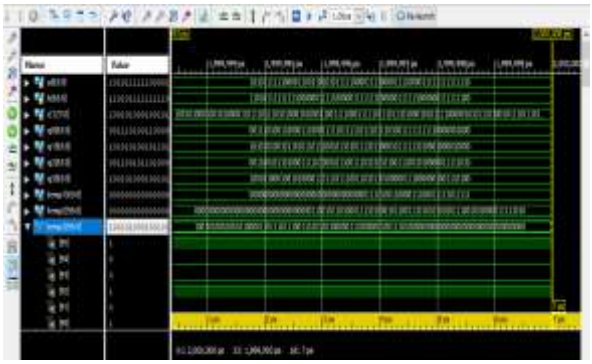

Figure 12 Values of internal signal temp3

Figure 13 Values of internal signal temp4

Figure 10, 11, 12 and 13 shows internal signal values of temp1, temp2, temp3 and temp4.

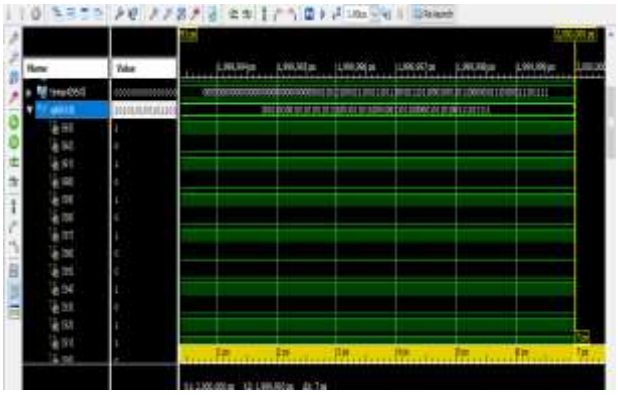

Figure 14 Values of internal signal q4

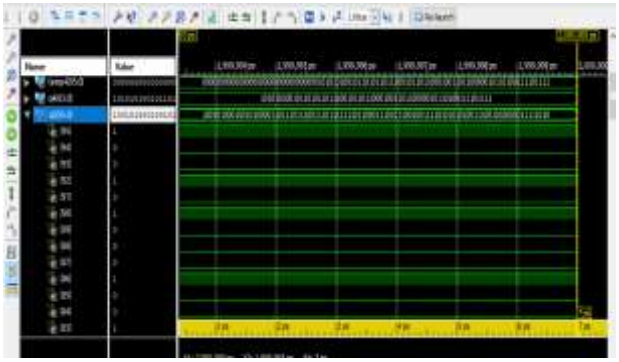

Figure 15 Values of internal signal q5

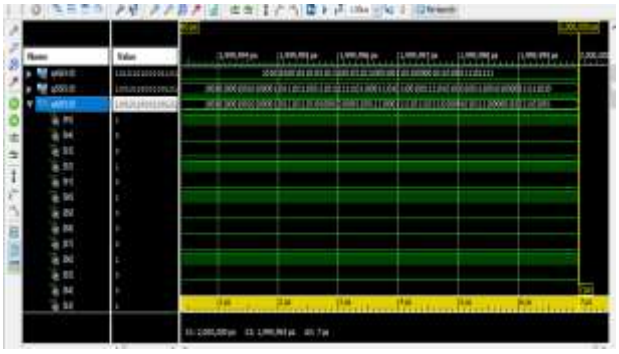

Figure 16 Values of internal signal q6

Figure 14, 15 and 16 shows internal signal values of q4, q5 and q6, which uses during simulation.

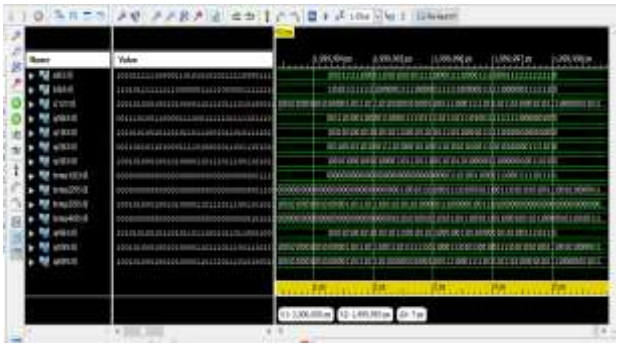

Figure 17 Output values during simulation

Figure 5.17 shows complete sub-module values of given input 'a' and input 'b'.

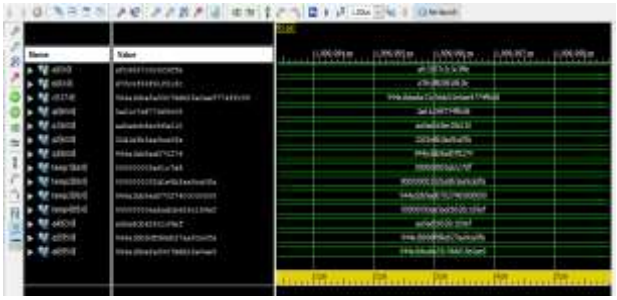

Figure 18 Output values during simulation in hexadecimal

V. RESULT AND PARAMETER CALCULATION

1. Area

Table 1 Device utilization summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	95	63400	0%
Number of fully used LUT-FF pairs	0	95	0%
Number of bonded IOBs	192	210	91%

Table 1 is showing summary of components using duration proposed booth multiplier implementation. Total number of slice look up table used 95 while availability is 63400. Look up table and flip flop pairs used 0 while availability is 95. Bonded input output block used 192 while availability is 210. Now total area is calculated from this utilization summary. Therefore, 30.33% area used for implementation of proposed 64 bit booth multiplier.

2. Power

Figure 19 X-power Analyzer

Table 2 is showing Xilinx power analyzer. Various family of FPGA IC like artix, kintex, spartan, vertex etc available. Input power and consume power is in milli W. Therefore, the total average consume power is booth 0.082mW.

Table 2 Primitive and Black Box Usage summary

Sr No.	Block Name	Quantity
1	BELS	95
2	LUT2	1
3	LUT3	31
4	LUT4	1
5	LUT5	60
6	LUT6	2
7	IO Buffers	192
8	IBUF	128
9	OBUF	64

3. Timing Analysis

Timing Constraint: Default path analysis
Total Number of Paths / Destination Ports: 4160 / 64
Total Delay: 13.745ns
Logic Delay: 3.105ns
Routing Delay: 10.640ns
Logic Proportion: 22.6%
Routing Proportion: 77.4%
All values displayed in nanoseconds (ns)

Cell	Fanout	Delay (ns)	Logic Delay (ns)	Logical Name (Net Name)
IBUF:I->O	2	0.001	0.698	input1_2_IBUF (input1_2_IBUF)
LUT6:I0->O	3	0.097	0.305	generate_N_bit_Adder[2].f/c_out1 (carry<2>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[4].f/c_out1 (carry<4>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[6].f/c_out1 (carry<6>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[8].f/c_out1 (carry<8>)
LUT3:I2->O	2	0.097	0.3	generate_N_bit_Adder[9].f/c_out1 (carry<9>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[11].f/c_out1 (carry<11>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[13].f/c_out1 (carry<13>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[15].f/c_out1 (carry<15>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[17].f/c_out1 (carry<17>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[19].f/c_out1 (carry<19>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[21].f/c_out1 (carry<21>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[23].f/c_out1 (carry<23>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[25].f/c_out1 (carry<25>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[27].f/c_out1 (carry<27>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[29].f/c_out1 (carry<29>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[31].f/c_out1 (carry<31>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[33].f/c_out1 (carry<33>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[35].f/c_out1 (carry<35>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[37].f/c_out1 (carry<37>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[39].f/c_out1 (carry<39>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[41].f/c_out1 (carry<41>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[43].f/c_out1 (carry<43>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[45].f/c_out1 (carry<45>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[47].f/c_out1 (carry<47>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[49].f/c_out1 (carry<49>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[51].f/c_out1 (carry<51>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[53].f/c_out1 (carry<53>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[55].f/c_out1 (carry<55>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[57].f/c_out1 (carry<57>)
LUT5:I4->O	3	0.097	0.305	generate_N_bit_Adder[59].f/c_out1 (carry<59>)
LUT5:I4->O	2	0.097	0.515	generate_N_bit_Adder[61].f/c_out1 (carry<61>)
LUT3:I0->O	1	0.097	0.279	generate_N_bit_Adder[62].f/Mxor_s_xo<0>1
OBUF:I->O	0	0	0	answer_62_OBUF (answer<62>)

Total Memory Usage: 4625700 kilobytes
Total Real Time to Xst Completion: 19.00 secs
Total CPU Time to Xst Completion: 19.27 secs

Table 3 Simulation Parameter

Sr No.	Parameters	Proposed Work
1	Type of Multiplier	64-bit Booth-Multiplier
2	Area	287
3	Total delay	3.10 ns
4	Accuracy rate	97%
5	Simulation Time	19.00 Secs
6	Power	8.2mW
7	PDP (Power delay product)	25.46
8	Frequency	322 MHz
9	Throughput	20.6 GHz
10	Memory	4625700 kilobytes
11	Global Maximum Fanout	100000

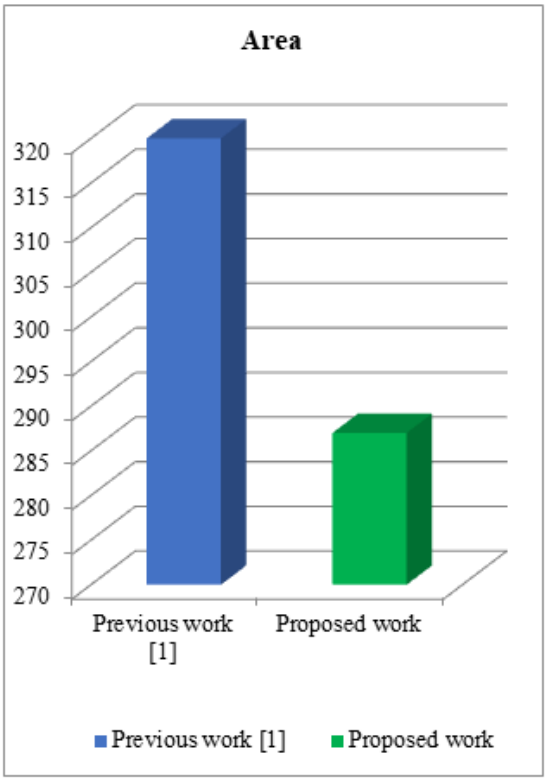

Figure 20 Comparison graph- Area

Table 4 Result Comparison

Sr No.	Parameters	Previous work [1]	Proposed work
1	Area	320	287
2	Delay	4.92 ns	3.105 ns
3	Power	9.13 mW	8.2mW
4	PDP (Power delay product)	44.91	25.46

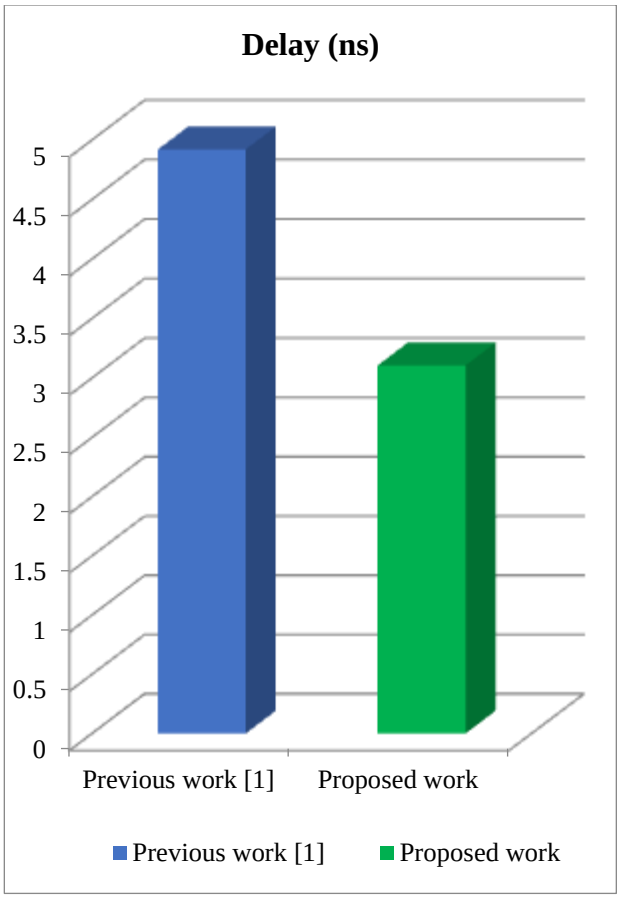

Figure 21 Comparison graph- delay

Therefore proposed 64-bit booth multiplier gives better result in term of calculated parameters. So, it can be used in high speed, low area and latency.

V. CONCLUSION

The Booth multiplier effectively identifies the operand serving as the multiplier and performs multiplication by reducing the number of addition steps compared to conventional methods. As a critical component in arithmetic processors, modern mobile applications and digital signal processing (DSP) require integrated circuits (ICs) that offer high-speed operations with low power consumption. This research presents an analysis of various performance metrics, including power, area, latency, throughput, frequency, and power-delay product, to identify optimal models for high-speed applications. It was determined that the power consumption of multipliers and the fundamental building blocks of CMOS VLSI circuits are closely

linked to the switching activities of adders. Consequently, a 64-bit efficient Booth multiplier was implemented and validated using Xilinx ISE 14.7 software. The design incorporates Booth half-adders, full-adders, and 4-2 compressors to enhance multiplier speed. The proposed multiplier demonstrates minimal loss in output quality while achieving significant savings in power and area.

The proposed 64x64-bit Booth multiplier emerges as one of the fastest options for FPGA-VLSI applications. Using the Virtex 5 and 7 family of FPGA ICs for simulation, the area utilized was reduced to 287 components from a previous count of 320. The delay was minimized to 0.344 ns, down from 4.92 ns in earlier designs. Power consumption decreased from 9.13 mW to 8.2 mW, and the power-delay product improved from 44.91 to 25.46 in the proposed design. These results indicate that the proposed Booth multiplier offers significant enhancements over existing implementations.

Future Scope

Booth processing has widespread applications in areas that are tolerant of errors, such as multimedia processing, artificial intelligence, signal processing, and real-time computing. Various applications in signal processing, computer vision, and AI exhibit inherent resilience to certain computational errors.

This error tolerance can be leveraged to trade off precision for reduced power consumption and area efficiency. Given that multiplication is a fundamental arithmetic operation in these applications, this work specifically focuses on enhancing this process with a robust Booth multiplier featuring a well-structured error distribution.

The multiplier can be designed to ensure that errors are evenly distributed, leading to lower computational inaccuracies in practical applications where errors tend to cancel each other out rather than accumulate, especially when the multiplier is employed repeatedly for calculations.

Future work could involve the implementation of Booth multipliers for 128-bit and 256-bit data multiplication.

Enhancements could be made to sub-modules such as compressors and carry-save adders to improve overall performance.

Furthermore, functional implementation in high-speed real-time digital multipliers remains a promising direction for continued research.

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