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Graphene-Based FET Prepared by Mechanical Exfoliation Technique for High-Performance

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Abstract- This study aims to prepare high-quality graphene using mechanical exfoliation and to fabricate a Field-Effect Transistor (FET) on a silicon substrate. The graphene's structural and electronic properties were evaluated through Raman spectroscopy, showing a prominent G Band (~1580 cm^{-1}) and 2D Band (~2700 cm^{-1}), indicating high-quality, monolayer graphene with low defect density. The transfer I-V characteristics reveal effective current modulation with high electron mobility, leading to faster switching speeds and lower power consumption. The Id-Vg characteristics demonstrate a distinct threshold voltage (0.75V) and highlight the importance of minimizing hysteresis for reliable device performance. The results confirm the efficacy of the exfoliation method in producing graphene suitable for high-performance FET applications.

Keywords- Graphene, exfoliation, FET, I-V characteristics, Raman spectrum

I. INTRODUCTION

Graphene, a single layer of carbon atoms arranged in a hexagonal lattice, has captivated the scientific community since its isolation due to its remarkable electronic, thermal, and mechanical properties. As an ideal candidate for next-generation electronic devices, Field-Effect Transistors (FETs) based on graphene offer unprecedented performance potential, including high electron mobility, flexibility, and transparency. However, synthesising high-quality graphene remains a formidable challenge, particularly when utilizing exfoliation techniques to achieve scalable and reproducible results. Exfoliating graphene from bulk graphite involves overcoming the van der Waals forces that hold the layers together, aiming to produce defect-free and high-purity graphene flakes. Various exfoliation techniques, such as mechanical, chemical, and electrochemical, have been explored to balance yield, quality, and efficiency. The focus of this research proposal is to optimize these exfoliation methods to produce graphene with superior electrical characteristics specifically tailored for FET applications. In light of the extensive research and theoretical models that delve into the unique electronic properties of graphene, it is evident that understanding the electronic band structure of graphene and addressing the hysteresis effect in graphene-based field-effect transistors (FETs) are fundamental to enhancing device performance. Some studies and theoretical models have advanced our comprehension of this critical aspect. One of them is called the Electronic Band Structure of Graphene. The unique band structure of graphene, characterized by massless Dirac fermions and a linear energy-momentum relationship, plays a pivotal role in its high electron mobility and exceptional electrical conductivity. Understanding this band structure is crucial for optimizing graphene-based devices, [1]. Hysteresis in Graphene FETs: Hysteresis in graphene FETs is a common phenomenon that affects device performance. Theoretical models like the Preisach model have been used to understand and mitigate hysteresis effects,[2]. The Commonly Cited Research was given by [3]. This paper discusses the electrical characterization and hysteresis effect of graphene

FETs fabricated using mechanically exfoliated graphene flakes. It highlights the importance of understanding hysteresis and p-doping in graphene devices[3]. Narayan and Kim produced a review article showcasing recent research progress and shortcomings of surfactant-assisted graphene LPE. It comprehensively assesses the quality and yield of graphene sheets produced by different surfactants [4]. The purpose of this work is to prepare high-quality graphene by exfoliation and fabricate the FET device on a silicon substrate. The study also investigates the electrical properties of the prepared device as the FET device offers crucial insights into the material's structural and electronic properties.

II. METHODS AND MATERIALS

The graphene samples were prepared using mechanical exfoliation and transferred to a silicon substrate with a 300 nm layer of thermally oxidized SiO2 on top (fig.1-a,b). The monolayer graphene was evaluated using an optical microscope and a Raman spectrometer[5,6]. the surface morphology of the device was characterized using an optical microscope and atomic force microscopy (AFM), [7]. The quality of the graphene channel was assessed through Raman spectroscopy using a 532nm laser. To ensure the removal of O2 and water molecules absorbed on the graphene surface, the samples underwent high vacuum cleaning. A 1 μm thick photoresist was applied, followed by spin-coating a 0.5 μm thick lift-off resist on the sample surface before adding another 0.5μm thick photoresist layer. Conventional photolithographic steps were then performed using a mask aligner to position the contacts accurately. For contact fabrication, a mask was designed to minimize damage from high-energy atoms.

A 40 nm layer of gold was deposited as contact material using a three-target RF diode and magnetron sputtering machine. The vacuum level during this process was maintained at 2×10^{-7} Torr, with an argon pressure of 3 mTorr for the deposition. Water cooling was employed throughout the sputtering process. Finally, changes in the electrical properties induced by exposure to air, thermal annealing in argon, thermal annealing in a vacuum, and chemical cleaning were analyzed using a Keithley 2600A source meter under ambient conditions, (Fig. 2).

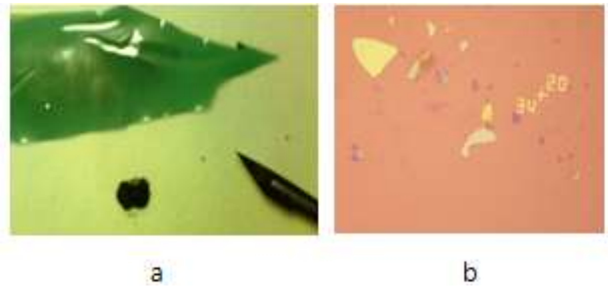

Figure 1: Preparation of the graphene by exfoliation method (a) and transferring them to a silicon substrate (b).

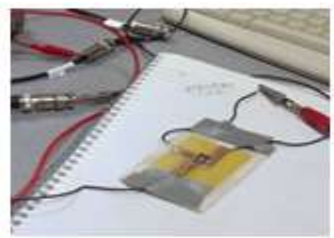

Figure 2: The FET device under test

III. RESULTS AND DISCUSSION

Fig. 3, shown the Raman spectrum. The G Band (Around 1580 cm^{-1}), its presence and intensity indicate the high quality of the graphene sample. A sharp and prominent G band peak confirms the graphene is composed of sp^2 hybridized carbon, which is critical for its electrical properties. 2D Band (Around 2700 cm^{-1}) is a second-order overtone of the D band and provides key information regarding the number of graphene layers. This peak is sharp and often more intense for single-layer graphene than the G band. Absence of D Band (Around 1350 cm^{-1}): While not explicitly shown in the provided spectrum, the D band indicates defects and disorder within the graphene lattice. This peak's absence or minimal presence suggests a low defect density, which is essential for achieving high electron mobility and superior electrical conductivity in graphene FET devices. The high-quality Raman spectrum, with distinct and well-defined G and 2D bands and the absence of the D band, underscores the effectiveness of the mechanical exfoliation method in producing high-quality monolayer graphene. This quality is paramount for the performance of FET devices, as it directly impacts electron mobility and overall efficiency.

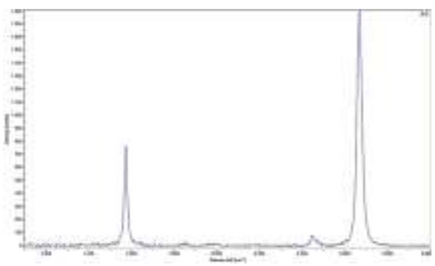

Figure 3: Raman spectrum for graphene prepared by exfoliation methods

Figure 4 shows the transfer I-V characteristics of (FET). The I-V curves show how the drain current varies with the drain voltage (Vd) for different gate-source voltages. As the gate-source voltage becomes more negative (e.g., from 0V to -1.0V), the drain current decreases for a given drain voltage. This indicates the FET's ability to modulate the current flow through the graphene channel, which is a fundamental characteristic of FET operation. The modulation capability is critical for the functioning of electronic devices as it allows precise control over the current.

Graphene's unique electronic properties, such as high electron mobility, are reflected in the I-V characteristics. The sharp response of the drain current to changes in the gate-source voltage demonstrates the efficiency of charge carrier modulation in the graphene channel. High electron mobility leads to faster switching speeds and lower power consumption in electronic devices. The I-V characteristics are crucial for optimizing the fabrication process and material quality. Any curve deviations or anomalies can indicate issues such as defects in the graphene layer, contact resistance, or impurities. By carefully analyzing the I-V curves, researchers can identify and address these issues to improve the overall performance and reliability of the FET.

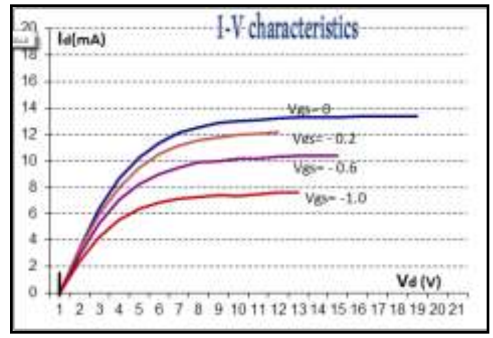

Figure 4: The transfer I-V characteristics of (FET)

From figure 5, one can say that the graph of drain current (Id) versus gate voltage (Vg) indicates how the current through the graphene channel changes in response to variations in the gate voltage. When a back gate voltage of 0.5V is applied, the Id-Vg curve shows a distinct transition point where the drain current increases sharply. This transition represents the threshold voltage (0.75V) at which the graphene channel starts to conduct significantly. The ability to control the drain current through the gate voltage is a fundamental characteristic of FET operation.

Graphene's intrinsic high electron mobility is reflected in the steep slope of the Id-Vg curve after the threshold voltage is reached. This steep increase in drain current with increasing gate voltage indicates that the graphene channel can effectively modulate charge carriers, leading to fast switching speeds and high conductivity. The Id-Vg characteristics typically exhibit two primary regions; linear and saturation regions. In the linear region, the drain current increases linearly with the gate voltage, indicating the resistive behavior of the channel. As the gate voltage increases, the device enters the saturation region, where the drain current levels off and becomes less dependent on the gate voltage. The point at which the Id-Vg curve shows a sharp increase in drain current is known as the threshold voltage (Vth). This voltage is critical for determining the operating conditions of the FET. In graphene-based FETs, the threshold voltage can be influenced by factors such as the quality of the graphene layer, the dielectric material used, and the device fabrication process. Accurately identifying and controlling the threshold voltage is important for optimizing device performance.

Hysteresis in the Id-Vg characteristics can occur due to charge trapping at the graphene-dielectric interface or other defects in the device. This phenomenon is observed as a difference in the Id-Vg curve during forward and reverse voltage sweeps. Minimizing hysteresis is crucial for ensuring consistent and reliable device performance. The back gate voltage of 0.5V influences the device's overall electric field distribution, affecting the graphene channel's charge carrier density. The back gate voltage also plays a role in controlling the threshold voltage and mitigating hysteresis effects.

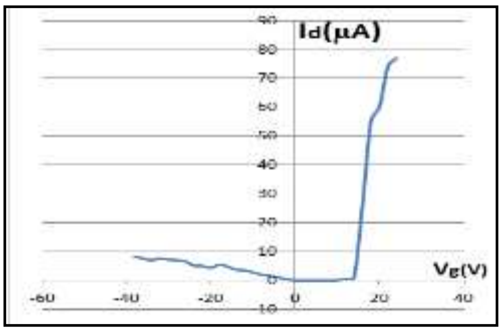

Figure 5: Id-Vg at 0.5mV curve for the electric properties for prepared FET

The Dirac point is the gate voltage (Vg) at which the drain current (Id) is at its minimum, indicating the transition from electron to hole conduction[8]. At the Dirac point, the graphene channel has equal probabilities for electrons and holes, leading to minimal current. So, Near the Dirac point, graphene exhibits high electron mobility, with rapid increases in current as Vg changes. Based on the provided image, the Dirac point appears to be located around Vg = 0 V. Precisely locating the Dirac point is crucial for tuning the electronic properties and optimizing the performance of graphene-based FET.

IV. CONCLUSION

Raman Spectrum Analysis indicate that the G Band Confirms high-quality, sp^2 hybridized carbon, and the 2D Band Indicates monolayer graphene with high electrical conductivity, where D Band: Absence suggests low defect density, ensuring high electron mobility. This is consistent with what was stated in [9 and 10].

Transfer I-V Characteristics: Demonstrates effective current modulation in the graphene channel with varying gate-source voltages. This reflects graphene's high electron mobility, which leads to faster switching speeds and lower power consumption. Also, Id-Vg Characteristics: Shows distinct threshold voltage (0.75V) for significant channel conduction.

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