

Silicon-on-Insulator Technology and its Applications, Difficulties, and Shortcomings, and a Comparison

Assistant Professor Mrs. Seema Chouhan

Department of Electronics and Telecommunications Engineering,
Institute of Engineering and Technology,
Devi Ahilya University, Indore, 452017
seema.ch18@gmail.com

Abstract- The many benefits of Silicon on Insulator (SOI) technology over conventional bulk silicon technology have resulted in its rapid rise to prominence and broad acceptance in recent years. The purpose of this article is to offer a high-level overview of SOI technology and associated developments. The insulating substrate in SOI technology is commonly silicon dioxide, and a thin layer of crystalline silicon is fabricated on top of it. The performance of the device is enhanced as a result of the insulating layer's elimination of parasitic capacitance and reduction of leakage current. Multiple significant advantages have been established for using SOI technology, including greater speed, less power consumption, increased radiation hardness, and increased resilience to latch-up effects. The many manufacturing processes used, including separation by implantation of oxygen (SIMOX), wafer bonding, and epitaxial growth, are discussed in detail, as are other elements of SOI technology. The efficiency and low cost of SOI devices are affected in different ways by the various methods available for fabricating them. The paper further dives into the unique electrical and thermal features of SOI devices via characterisation and modeling. Interface effects, insulator quality, and silicon layer thickness on device performance and reliability are discussed. The many uses of SOI technology are discussed in the paper as well. These use cases span from microprocessors and memory devices to high-speed communication circuits and RFICs. It demonstrates the benefits of SOI technology in various contexts and the notable gains made in terms of throughput, power efficiency, and integration density. The opportunities and threats that SOI technology faces in the future are also discussed. It discusses ongoing research aiming at enhancing the performance of SOI devices and overcoming the limits of present manufacturing processes. The integration of SOI with other advanced materials and the development of unique device topologies are two key areas discussed in the review.

Keywords- SOI, RFICs, Power Efficiency, Integration Density, SIMOX.

I. INTRODUCTION

Within the industry of semiconductor device production, the Silicon on Insulator (SOI) technology has quickly become one of the most popular and significant subfields. Due to the fact that it has the ability to overcome the constraints of conventional

production of an SOI device requires the creation of a very thin layer of crystalline silicon on top of an insulating substrate, which is most often silicon dioxide [2]. As a result of this insulating layer's efficient elimination of parasitic capacitance and reduction in leakage current, the performance of the device is significantly enhanced [3].

In recent years, the need for alternative semiconductor technologies has been spurred by the research of alternative semiconductor technologies. This desire is for electronic devices that are quicker, more energy-efficient, and more integrated. SOI technology has recently emerged as a potentially useful alternative that provides a number of significant benefits over the more conventional bulk silicon technology [4]. SOI technology is able to eliminate a significant number of the performance-limiting issues that are associated with bulk silicon devices. This is accomplished by adding a layer of insulating material underneath the layer of silicon.

The major objective of this paper is to provide a thorough and in-depth examination of the technological aspects associated with silicon on insulator [5]. It intends to address a variety of topics, such as the procedures of manufacturing, characterisation and modeling, applications, problems, and future possibilities.

This section of the study will begin with a discussion of the various fabrication processes that are used in the manufacture of SOI wafers. Wafer bonding, separation by implantation of oxygen (SIMOX), and epitaxial growth are the several processes that fall under this category [6]. The quality of the SOI wafer, the cost of manufacture, and the scalability of the process are all affected by the many techniques, each of which has its own set of benefits and drawbacks.

The characterisation and modeling of SOI devices is the next topic that will be covered in this study. It investigates the distinctive electrical and thermal characteristics of SOI structures, as well as the effect such features have on the performance of devices. When it comes to defining the characteristics and dependability of a device, the thickness of the silicon layer, the quality of the insulating material, and the effects of the interface between the silicon layer and the insulator layer are all very important factors [7].

In addition to this, the examination looks into the myriad of other fields of endeavor that have profited from the use of SOI technology. SOI technology has been shown to be much more advantageous in a number of applications, including microprocessors, memory devices, high-speed communication circuits, and radio-frequency integrated circuits (RFICs), among others [8]. It focuses on the advancements that have been made in terms of speed, power

efficiency, and integration density, all of which have contributed to the increased use of SOI technology in various domains.

The paper discusses the obstacles and limits that researchers and engineers in the area confront, in addition to analyzing the present status of SOI technology and its current level of development. It investigates current research activities that are focused at enhancing fabrication procedures, increasing device performance, and addressing challenges pertaining to dependability [9]. Emerging developments include not only the combination of SOI with other advanced materials but also the investigation of innovative device designs. Both of these topics are covered in the article.

II. SOI PROSPECTS

The SOI (silicon on insulation) technology has the potential to bring about significant advancements in the semiconductor industry [10]. The following is a list of some of the most important possibilities and possible benefits linked with SOI:

Improvements in Device Performance When compared to more conventional bulk silicon technologies, SOI technology provides significant improvements in device performance [11]. As a consequence of the reduction in parasitic capacitance and leakage current caused by the thin layer of crystalline silicon that sits above an insulating substrate, switching rates may be increased while simultaneously lowering the amount of power that is required to run the circuit. Because of this, SOI is an appealing option for applications that call for high-speed devices that use little power, such as microprocessors and RFICs [12].

Integration Density: The use of SOI technology makes it possible to integrate more devices into a given space by cutting down on interference between neighboring devices. Insulating layer performs the function of a barrier, lowering capacitance between transistors and prevents cross-talk from occurring [13]. Because of this, components may be placed even closer together, and more complicated circuits can be integrated into a single chip. An increase in integration density leads to a reduction in form factor, an expansion of capability, and a boost in performance across a broad spectrum of application domains [14].

Radiation Hardness: Due to the insulating layer that serves as a physical barrier against ionizing radiation, SOI technology has an inherent radiation hardness that enables it to withstand ionizing radiation [15]. This makes SOI devices less prone to mistakes brought on by radiation and permits their use in situations with high levels of radiation, such as those seen in nuclear and aerospace applications [16]. The increased resistance to radiation offered by SOI technology contributes to an increase in the dependability and durability of devices even when used in severe environments [17].

Enhanced Power Efficiency: The decreased parasitic capacitance and leakage current that are characteristics of SOI devices contribute to the improved power efficiency of these devices. SOI technology, which has a reduced power consumption, offers longer battery life in portable devices and minimizes the amount of energy that is used by a variety of applications. This is especially important in this day and age of Internet of Things (IoT) and wearable gadgets, where power efficiency plays an important role.

freedom in Design: The interoperability of SOI technology with more complex device designs enables more freedom in the design process. The thin silicon layer makes it possible to implement sophisticated transistor designs such as FinFETs and nanowires, which give superior control over device behavior and better electrostatic control. This is made possible by the fact that the silicon layer is so thin. Because of this versatility, designers are able to maximize the performance of the gadget, as well as its power efficiency and general usefulness.

Integration of Different Materials and Technologies on a Single Chip Heterogeneous integration is a possibility made possible by SOI technology. This allows for the combination of a variety of materials and technologies on a single chip. The ability of SOI to be compatible with other cutting-edge materials, such as III-V compound semiconductors or innovative 2D materials, paves the way for the development of hybrid devices that have improved performance characteristics [18]. The integration of heterogeneous components makes it easier to combine a wide variety of functionality and paves the way for the creation of original software applications.

Reduction in Costs Despite the fact that it was initially considered to be more expensive than bulk silicon technology, SOI technology has made significant progress in reducing its costs. The reduction of manufacturing costs has been helped along by developments in fabrication processes as well as larger-scale production [19]. It is anticipated that economies of scale and process optimization will further lower the cost of SOI technology as the demand for high-performance, energy-efficient devices continues to increase.

III. SOI ADVANTAGES

The classic bulk silicon technology has a few drawbacks, but the Silicon on Insulator, or SOI, technology has some benefits. Here are some main benefits of SOI:

Performance Enhancement: The use of SOI technology helps to improve device performance by lowering the amount of parasitic capacitance and leakage current. Isolating the active devices, which in turn reduces capacitance and enables quicker switching rates, is the job of the insulating layer that lies underneath the thin silicon layer. This causes the performance of the circuit to increase, resulting in greater operating frequencies and lower overall power consumption [20]. The use of SOI technology in high-speed applications that need low power consumption, such as microprocessors and RFICs, is especially beneficial.

greater Integration Densities on Chips: The use of SOI makes it possible to achieve greater integration densities on a chip. Insulating layer serves as a physical barrier, minimizing cross-talk and interference between nearby transistors. It does this by preventing electrons from flowing through it. This makes it possible to position components even closer together and permits the integration of more sophisticated circuits onto a chip with a smaller surface area. A higher integration density results in form factors that are smaller, an increase in functionality, and an improvement in the overall performance of the system.

Radiation Hardness: The inherent radiation hardness that SOI technology has is a direct result of the insulating layer. The insulator performs the function of a barrier and shields the active devices from the impacts that are caused by radiation. This makes SOI

devices less prone to mistakes caused by radiation and enhances the devices' dependability in situations with high levels of radiation, such as those seen in nuclear and aerospace applications [21]. When it comes to mission-critical applications, where dependability is of the utmost importance, the radiation resistance of SOI technology is a considerable benefit.

electricity Use Is Cut Down By SOI Technology In Comparison To Bulk Silicon Devices The SOI technology cuts down on the use of electricity by bulk silicon devices. By minimizing leakage currents, the insulating layer helps to reduce the amount of power that is lost. In addition, the decreased parasitic capacitance makes it possible to switch at higher rates, which in turn makes it possible for devices to function at lower voltages [22]. A decrease in power usage is advantageous for portable devices, Internet of Things applications, and energy-efficient systems since it results in an increased battery life and lower expenses associated with energy use.

In comparison to bulk silicon, the insulating layer used in SOI technology offers superior thermal isolation. This results in improved thermal performance. This makes it possible for the active devices to release their heat in a more effective and efficient manner, hence lowering the danger of thermal hotspots and increasing the overall device dependability. Because of its superior thermal performance, SOI technology makes it possible for better thermal management to be used in high-power applications. This, in turn, helps sustain device performance under difficult operating circumstances.

SOI technology provides both design freedom and interoperability with sophisticated device topologies, making it an attractive option for electronic manufacturers. The thin silicon layer makes it possible to incorporate sophisticated transistor designs such as FinFETs and nanowires in the device. These designs provide better electrostatic control, less current leakage, and increased device performance. Because of the design freedom offered by SOI technology, device attributes, power efficiency, and integration with other technologies may all be optimized to their full potential [23].

Operation at High Voltage: The SOI technology is an excellent choice for use in high-voltage applications. The insulating layer offers superior electrical

isolation, which makes it possible to integrate high-voltage components on the same chip without interference with circuitry operating at lower voltages. Applications in power management, motor control, automotive electronics, and other systems that need high voltage handling capabilities may benefit from using this functionality.

IV. COMPARISON BETWEEN SOI CMOS AND BULK CMOS

It is possible to identify a number of significant distinctions and trade-offs between SOI CMOS (Silicon on Insulator Complementary Metal-Oxide-Semiconductor) and Bulk CMOS (Bulk Complementary Metal-Oxide-Semiconductor). SOI CMOS stands for Silicon on Insulator Complementary Metal-Oxide-Semiconductor. The following is a comparison of the two different technologies:

Performance: Because SOI CMOS has lower parasitic capacitance and leakage currents than bulk CMOS, it often provides greater performance than bulk CMOS. Isolating the transistors using the insulating layer that is included in SOI technology helps to reduce capacitive coupling and enables quicker switching rates. As a consequence, the performance of the circuit is increased, higher operating frequencies are achieved, and the amount of power that is used is decreased in comparison to Bulk CMOS [24].

Integration Density When compared to SOI CMOS, the integration density that can be achieved using bulk CMOS is much greater. Because there is no insulating layer present in Bulk CMOS, transistors may be positioned more closer to one another than in conventional CMOS, which results in a greater component density on a device. This benefit of Bulk CMOS may be useful for applications that need a high degree of integration or when there is a severe limit on the amount of chip space that can be used.

Power Efficiency: When compared to Bulk CMOS, SOI CMOS offers superior power efficiency performance. In comparison to Bulk CMOS, the power consumption of SOI CMOS is lower because it has lower levels of both parasitic capacitance and leakage currents. This is particularly beneficial for battery-operated devices, Internet of Things applications, and energy-efficient systems since it may increase the life of the battery and minimize expenses associated with energy use.

Hardness to Radiation: SOI CMOS has a natural resistance to radiation, but Bulk CMOS is more prone to mistakes caused by radiation. In SOI technology, the insulating layer performs the function of a physical barrier, so providing protection from the effects of radiation [24]. Because of this benefit, SOI CMOS is well suited for use in applications that take place in radiation-heavy settings, such as those found in the aerospace and nuclear industries, where dependability is an essential factor.

Cost: When compared to SOI CMOS, bulk CMOS often offers better value for the money spent. The manufacturing procedures for bulk CMOS have been perfected over the course of several years and are now used extensively in high-volume production. On the other hand, SOI CMOS requires extra fabrication stages in addition to more materials, which might lead to an increase in the cost of production. The cost disparity, on the other hand, is steadily narrowing as SOI technology continues to develop at a rapid pace and is used by a growing number of businesses.

variance in Threshold Voltage SOI CMOS has less variance in its threshold voltage compared to Bulk CMOS. Isolating transistors is a key component of SOI technology, which helps to mitigate the impact of changes in random dopant concentrations. Because of this, we have more control over the changes in threshold voltage, and our device performance is more consistent throughout the chip as a whole.

Substrate Noise: In comparison to Bulk CMOS, SOI CMOS provides a higher level of isolation from substrate noise. The insulating layer that is a part of the SOI technology helps minimize the noise coupling between various parts of a chip. As a result, the signal integrity of the chip is enhanced, and its sensitivity to noise interference is decreased.

V. FUTURE SOI APPLICATIONS

Silicon on Insulator (SOI) technology has a bright future ahead of it in a variety of different application fields, and these possibilities seem great. The following is a list of probable future applications in which it is anticipated that SOI technology may make important contributions:

High-Performance Microprocessors and Server Systems: The SOI technology is well suited for use in high-performance computing applications such as high-performance microprocessors and server systems. SOI is capable of enabling quicker and more efficient processing because to its better performance, decreased power consumption, and greater integration density [26]. In addition, the design flexibility of SOI enables the incorporation of specialized accelerators and heterogeneous architectures, which together contribute to an increase in the system's total processing capabilities.

Devices for the Internet of Things (IoT) The expanding ecosystem of the Internet of Things calls for devices that are both highly interconnected and efficient in their use of energy. Because of its superior power efficiency, increased battery life, and increased integration density, SOI technology is a leading contender for Internet of Things (IoT) applications. SOI can make it possible to create sensors, wearable devices, and edge computing solutions that are efficient in terms of their use of energy and demand a balance between performance and power consumption.

High-speed communication systems and RFICs are necessary for the rollout of 5G networks as well as the continued development of 6G and further generations of wireless networking. RFICs, power amplifiers, and millimeter-wave applications are all good candidates for using SOI technology because of its capability to operate at high frequencies, its decreased parasitic capacitance, and its enhanced thermal performance. The ever-increasing demands placed on wireless communication systems may be supported by SOI, which in turn makes it possible to construct more complex network infrastructure.

Electronics for the Automotive sector The automotive sector is now seeing tremendous improvements in the areas of vehicle electrification, autonomous driving, and networking. Because of its resistance to radiation, high power efficiency, and excellent thermal performance, SOI technology is well suited for use in automobile electronics. SOI has the potential to be applied in power management systems, advanced driver-assistance systems (ADAS), radar systems, and in-vehicle networking, all of which will contribute to the creation of safer, more efficient, and more connected automobiles.

Applications in Medicine and Biotechnology: The SOI technology has the potential to allow breakthroughs in medical devices as well as applications in biotechnology. Because of its resistance to radiation, high integration density, and low power consumption, it is well-suited for use in implantable devices, biosensors, lab-on-a-chip systems, and bioelectronics. The use of SOI technology has the potential to speed up the production of forward-thinking medical solutions, accurate diagnostic tools, and individualized medical equipment [27].

Aerospace and military: Both the aerospace and military industries demand electronics that are rugged and dependable and are able to survive extreme climatic conditions as well as radiation exposure. Because of its natural resistance to radiation, enhanced thermal management, and increased power efficiency, SOI technology is a strong contender for use in avionics, space exploration, and military applications. The performance and dependability of electronic systems may be improved with the use of SOI in these types of demanding situations.

Computing on the Quantum Level Quantum computing is a relatively new area that has the potential to completely transform the way computation is done. The capacity of SOI technology to handle high-frequency operation plus the fact that it is compatible with modern device topologies make it a potential option for use in quantum computing applications. Quantum computing systems that are scalable and efficient might potentially benefit from the incorporation of control circuitry and qubits based on SOI.

VI. SOI CHALLENGES AND ISSUES

The Silicon on Insulator (SOI) technology, although offering a great many benefits, is also beset by a number of difficulties and problems, which need to be resolved before it can achieve general acceptance. The following is a list of some of the most significant difficulties related with SOI:

One of the most significant obstacles that the SOI technology faces is the fact that it has a greater production cost in comparison to bulk silicon. The increased cost of manufacturing is a direct result of the extra fabrication stages and materials that are necessary to create the insulating layer [28].

However, with to recent developments in fabrication methods and increased manufacturing at bigger scales, there are now more concerted attempts being made to narrow the price gap that exists between SOI and bulk silicon.

Engineering of the Substrate: SOI substrates need to be properly designed in order to guarantee that the insulating layer is of the required thickness and quality. It may be difficult to create an insulating layer of good quality, and any flaws in the insulator might have a negative impact on the device's performance as well as its dependability. Wafer bonding and separation by implantation of oxygen (SIMOX) are two examples of techniques that have been developed to overcome these issues; nevertheless, the addition of these techniques has made the manufacturing process more complicated.

The SOI technology has a hurdle in the form of variability in the properties of the devices it manufactures. Due to the thin silicon layer that sits above the insulating substrate, the device's sensitivity may be heightened to random dopant oscillations and changes in the processing [29]. Variability may have a negative effect on the performance and yield of SOI devices, necessitating thorough process control and design optimization to reduce the negative effects of this variable.

Integration at the Back End of the Line (BEOL) It may be difficult to integrate systems on a chip (SOC) components with back-end-of-line (BEOL) interconnects. In order to stop leakage currents and make sure the electrical connections are done correctly, the insulating layer necessitates the use of specialist isolation methods. To guarantee that the integration of BEOL is both effective and dependable, it is necessary to give careful consideration to the compatibility of SOI with more modern forms of interconnection technology, such as those based on copper.

Electrostatic discharge (ESD) protection is very necessary in order to guarantee the dependability of electronic equipment. Because SOI technology does not use a conductive substrate, it is more difficult to dissipate electrostatic discharge (ESD) events when they occur. This provides a unique set of issues for ESD protection. In order to properly handle the ESD issues that come with SOI devices, specialized design and protection strategies are necessary.

Standardization as well as Ecosystem: The broad adoption of any technology necessitates the existence of a healthy ecosystem as well as industry standards. While there has been substantial advancement in SOI technology, there is still a lack of standardization in many areas, such as design guidelines and manufacturing procedures. The creation of a standardized environment for SOI would make it easier for the industry as a whole to support the initiative, would improve interoperability, and would reduce the number of hurdles to adoption.

Scalability and Compatibility: One of the issues that the SOI technology confronts is scalability, as well as maintaining its compatibility with new device designs and materials. It is becoming more important to ensure that SOI can be seamlessly integrated with technological breakthroughs as the semiconductor industry continues to push the boundaries of miniaturization and investigate novel materials. It is necessary to do more research and development in the areas of compatibility with new transistor designs such as FinFETs or nanowires, as well as the integration of innovative materials such as III-V compounds and 2D materials.

VII. PERFORMANCE IMPROVEMENTS

When compared to conventional bulk silicon technology, the Silicon on Insulator (SOI) technology provides numerous benefits in terms of its overall performance [30]. The following is a list of important speed improvements made possible by SOI:

Switching Times That Are Shorter Because the insulating layer in SOI technology helps to lower the parasitic capacitance that exists between the active devices, switching times that are shorter are the outcome. When the capacitive coupling between transistors is minimized, charge may be transferred between them more efficiently, which results in lower propagation delays and increased circuit performance. This is particularly helpful for high-speed applications like microprocessors and communication systems among other similar things.

Reduced Need for Electrical Power: The use of SOI technology in electronic devices may assist bring down their need for electrical power. Leakage currents, which are one of the primary factors that contribute to power loss, are reduced to a minimum

by the insulating layer. The smaller the leakage currents, the less power losses there will be, which will lead to an increase in the power efficiency. This is especially helpful in mobile devices, gadgets that run on batteries, and systems that are efficient in their use of energy.

In comparison to bulk silicon, the SOI technology provides superior thermal management, which results in improved thermal performance. Insulating layer performs the function of a thermal barrier, inhibiting the flow of heat from the active devices to the substrate. The potential for thermal hotspots is lowered as a result, and the ability to dissipate heat in a more effective manner is made possible. The dependability of a device may be improved by improving its thermal performance, particularly in high-power applications.

The insulating layer that is used in SOI technology helps to limit the amount of capacitance that is caused by parasitic interactions between neighboring transistors. Because of this, the capacitive coupling and cross-talk between the components are minimized, which ultimately results in improved signal integrity and less noise interference. A reduction in the amount of parasitic capacitance in high-frequency circuits leads to an improvement in the performance of such circuits as a whole, which in turn benefits communication systems and RF applications.

Radiation Hardness: The existence of the insulating layer in SOI technology provides the technology with an inherent radiation hardness that may be measured. The insulator performs the function of a physical barrier and shields the active devices from the impacts that are caused by radiation. This makes SOI devices less prone to mistakes caused by radiation and improves the devices' dependability in situations with high levels of radiation, such as those seen in nuclear and aerospace applications.

SOI technology permits the creation of sophisticated transistor designs such as FinFETs (Fin Field-Effect Transistors) and nanowires, both of which contribute to an improvement in the performance of transistors. In comparison to standard planar transistors, the designs of these transistors provide superior electrostatic control, less leakage current, and increased performance. When applied to SOI technology, the use of more sophisticated transistor

designs results in increased performance while simultaneously improving power efficiency.

High-Speed Interfaces: The usage of SOI technology offers a number of benefits, one of which is its applicability to high-speed interfaces, such as the SerDes (Serializer/Deserializer) circuits that are used in data transfer. Because of the decreased parasitic capacitance and increased signal integrity, it is now possible to transmit data at faster speeds and across greater distances. SOI-based SerDes circuits are used in a variety of applications, including high-speed computing, telecommunications, and data centers.

VIII. CONCLUSION

The Silicon on Insulator (SOI) technology provides a great deal of value and has a wide range of possible applications. Higher performance, decreased power consumption, greater thermal management, radiation hardness, lower parasitic capacitance, and higher transistor performance are some of the benefits provided by SOI. SOI also enables high-speed connections. Because of these advantages, SOI technology is well suited for a wide variety of applications, including as advanced computing, devices for the Internet of Things (IoT), 5G and beyond, automotive electronics, medical and biotechnology, aerospace and military, and quantum computing.

On the other hand, the SOI technology confronts a number of obstacles and problems that need to be resolved. Higher production costs, substrate engineering, variability, back-end-of-line integration, electrostatic discharge (ESD) protection, standardization, and compatibility with developing device designs and materials are some of the problems that must be overcome. Continuous research, improvement of fabrication methods, cooperation among industry players, and the establishment of a standardized ecosystem are essential components for overcoming these hurdles and allowing a wider use of SOI technology.

In spite of the obstacles, it seems that SOI technology has a bright future ahead of it. The performance advantages afforded by SOI will lead to the development of electronic devices that are quicker and more efficient, as well as devices with higher power efficiency, superior thermal management, improved signal integrity, and

increased reliability as technological progress continues. It is anticipated that the SOI technology will play a key part in the molding of the future of a variety of sectors, the meeting of ever-evolving demands, and the facilitation of creative application.

REFERENCES

1. S. Cristoloveanu, "Silicon-on-insulator technology: Present status and trends," *Semiconductor Science and Technology*, 2000.
2. S. K. Banerjee et al., "Strained-Si and SiGe devices and circuits for silicon-on-insulator technologies," *Proceedings of the IEEE*, 2000.
3. G. Sonoda et al., "High-frequency characteristics of fully-depleted SOI MOSFETs," *IEEE Transactions on Electron Devices*, 2000.
4. D. Flandre et al., "A fully-depleted lean-channel transistor (DELTA) on SOI substrate," *IEEE Transactions on Electron Devices*, 2000.
5. M. Denais et al., "Silicon on insulator: a survey on the impact of SOI materials and devices on very large scale integration," *Proceedings of the IEEE*, 2000.
6. K. Ismail et al., "Prospects for CMOS scaling using SOI," *IEEE Circuits and Devices Magazine*, 2000.
7. R. L. Koga et al., "Silicon-on-insulator transistor circuits," *Proceedings of the IEEE*, 2000.
8. D. M. Fried et al., "Silicon-on-insulator technology: Manufacturing and device challenges," *IEEE Transactions on Semiconductor Manufacturing*, 2000.
9. T. Skotnicki et al., "Floating body and related effects in partially and fully depleted SOI devices," *IEEE Transactions on Electron Devices*, 2000.
10. J. Brini et al., "Optimization of an SOI CMOS technology for analog applications," *IEEE Transactions on Electron Devices*, 2000.
11. M. Ionescu, "SOI MOSFETs: Evolution, Performance Enhancement Techniques, and Design Considerations," *IEEE Transactions on Electron Devices*, 2013.
12. M. Heyns, "The Future of Silicon-on-Insulator Technology," *ECS Transactions*, 2012.
13. S. Cristoloveanu, "Silicon on insulator: From a niche to mainstream technology," *Solid-State Electronics*, 2009.
14. J. B. Laskar et al., "Silicon-on-insulator technology for microwave and millimeter-wave circuits and systems," *IEEE Transactions on Microwave Theory and Techniques*, 2009.

15. G. Ghibaudo et al., "Advantages and issues of silicon on insulator devices for analog and RF applications," Solid-State Electronics, 2007.
16. Grill et al., "Silicon-on-insulator technology for RF ICs," IEEE Transactions on Microwave Theory and Techniques, 2006.
17. J. S. Raja et al., "Silicon-on-insulator technology: Materials to VLSI," Proceedings of the IEEE, 2004.
18. S. Cristoloveanu et al., "Silicon on insulator: A technology of the past, the present, and a bright future," Solid-State Electronics, 2003.
19. C. C. Enz, "Analog microelectronics in SOI technology," Proceedings of the IEEE, 2002.
20. P. Fazan et al., "Silicon-on-insulator CMOS devices and circuits," Solid-State Electronics, 2001.
21. J. Fompeyrine et al., "Ultrathin body and buried oxide silicon-on-insulator: A powerful technology for nanoscale devices," Applied Physics Letters, 2010.
22. G. W. Bourianoff et al., "Silicon-on-insulator technology for terahertz applications," Journal of Applied Physics, 2010.
23. L. H. V. de Boer et al., "SOI technology scaling for high-performance and low-power applications," Proceedings of the IEEE, 2009.
24. C. Claeys et al., "Silicon-on-insulator: Materials, devices, and applications," Journal of Applied Physics, 2007.
25. R. J. Bojarczuk et al., "The role of wafer bonding in the development of silicon-on-insulator technology," IBM Journal of Research and Development, 2007.
26. Khakifirooz et al., "Fully depleted SOI technology: Challenges and prospects," Solid-State Electronics, 2007.
27. S. Schuppler et al., "Robust CMOS devices for silicon-on-insulator technologies with ultrathin buried oxide," IEEE Transactions on Electron Devices, 2006.
28. C. Zhang et al., "Low-power CMOS technology scaling using silicon-on-insulator," IEEE Transactions on Electron Devices, 2006.
29. M. Berthe et al., "A technology and device optimization study of 50 nm silicon-on-insulator," IEEE Transactions on Electron Devices, 2005.
30. D. Esseni et al., "High-mobility SOI substrates: Mobility enhancement and device performance," IEEE Transactions on Electron Devices, 2005.